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Design of Adaptive Analog Filters for Magnetic Front-End Read Channels

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à minha família

”Era” *– a set of years, which is counted from a particular event or named after an important development: compare* Epoch...

The computer euphoria of modern times is self-evident. The computer has invaded the world, and will soon outnumber mankind. It has entered our quotidian lives, everywhere and inevitably, moreover computer assisted work is becoming the only form of work. Therefore it is natural that many call this the *computer era*.

Many have taken it as their subject of study, this work will be focused on the information storage process, namely on magnetic hard disk drives.

Sumário

Esta tese estuda o projecto e o comportamento de filtros em tempo contínuo de muito-alta-frequência. A motivação deste trabalho foi a investigação de soluções de filtragem para canais de leitura em sistemas de gravação e reprodução de dados em suporte magnético, com custos e consumo (tamanho total inferior a 1 mm^2 e consumo inferior a 1mW/polo), inferiores aos circuitos existentes. Nesse sentido, tal como foi feito neste trabalho, o rápido desenvolvimento das tecnologias de microelectrónica suscitou esforços muito significativos a nível mundial com o objectivo de se investigarem novas técnicas de realização de filtros em circuito integrado monolítico, especialmente em tecnologia CMOS (*Complementary Metal Oxide Semiconductor*). Apresenta-se um estudo comparativo a diversos níveis hierárquicos do projecto, que conduziu à realização e caracterização de soluções com as características desejadas.

Num primeiro nível, este estudo aborda a questão conceptual da gravação e transmissão de sinal bem como a escolha de bons modelos matemáticos para o tratamento da informação e a minimização de erro inerente às aproximações na conformidade aos princípios físicos dos dispositivos caracterizados.

O trabalho principal da tese é focado nos níveis hierárquicos da arquitectura do canal de leitura e da realização em circuito integrado do seu bloco principal – o bloco de filtragem. Ao nível da arquitectura do canal de leitura, apresenta-se um estudo alargado sobre as metodologias existentes de adaptação de sinal e recuperação de dados em suporte magnético. Este desígnio aparece no âmbito da proposta de uma solução de baixo custo, baixo consumo, baixa tensão de alimentação e baixa complexidade, alicerçada em tecnologia digital CMOS, para a realização de um sistema DFE (*Decision Feedback Equalization*) com base na igualização de sinal utilizando filtros integrados analógicos em tempo contínuo.

Ao nível do projecto de realização do bloco de filtragem e das técnicas de implementação de filtros e dos seus blocos constituintes em circuito integrado, concluiu-se que a técnica baseada em circuitos de transcondutância e condensadores, também conhecida

como filtros *gm-C* (ou transcondutância-C), é a mais adequada para a realização de filtros adaptativos em muito-alta-frequência. Definiram-se neste nível hierárquico mais baixo, dois subníveis de aprofundamento do estudo no âmbito desta tese, nomeadamente: a pesquisa e análise de estruturas ideais no projecto de filtros recorrendo a representações no espaço de estados; e, o estudo de técnicas de realização em tecnologia digital CMOS de circuitos de transcondutância para a implementação de filtros integrados analógicos em tempo contínuo.

Na sequência deste estudo, apresentam-se e comparam-se duas estruturas de filtros no espaço de estados, correspondentes a duas soluções alternativas para a realização de um igualador adaptativo realizado por um filtro contínuo passa-tudo de terceira ordem, para utilização num canal de leitura de dados em suporte magnético.

Como parte constituinte destes filtros, apresenta-se uma técnica de realização de circuitos de transcondutância, e de realização de condensadores lineares usando matrizes de transístores MOSFET para processamento de sinal em muito-alta-frequência realizada em circuito integrado usando tecnologia digital CMOS submicrométrica. Apresentam-se métodos de adaptação automática capazes de compensar os erros face aos valores nominais dos componentes, devidos às tolerâncias inerentes ao processo de fabrico, para os quais apresentamos os resultados de simulação e de medição experimental obtidos.

Na sequência deste estudo, resultou igualmente a apresentação de um circuito passível de constituir uma solução para o controlo de posicionamento da cabeça de leitura em sistemas de gravação/reprodução de dados em suporte magnético. O bloco proposto é um filtro adaptativo de primeira ordem, com base nos mesmos circuitos de transcondutância e técnicas de igualação propostos e utilizados na implementação do filtro adaptativo de igualação do canal de leitura.

Este bloco de filtragem foi projectado e incluído num circuito integrado (Jaguar) de controlo de posicionamento da cabeça de leitura realizado para a empresa ATMEL em Colorado Springs, e incluído num produto comercial em parceria com uma empresa escocesa utilizado em discos rígidos amovíveis.

Palavras-chave: filtros contínuos adaptativos, comparação de estruturas de filtros, igualação de sinal, tecnologia digital CMOS, processamento de sinal em corrente, circuitos de transcondutância CMOS, baixo consumo, muito-alta-frequência, área reduzida, baixo custo, baixa complexidade.

Abstract

This thesis studies the design and behavior of continuous-time very-high-frequency filters. The motivation of this work was the search for filtering solutions for the read-channel in recording and reproduction of data on magnetic media systems, with costs and consumption (total size less than 1 mm^2 and consumption under 1mW/pole), lower than the available circuits. Accordingly, as was done in this work, the rapid development of microelectronics technology raised very significant efforts worldwide in order to investigate new techniques for implementing such filters in monolithic integrated circuit, especially in CMOS technology (Complementary Metal Oxide Semiconductor). We present a comparative study on different hierarchical levels of the project, which led to the realization and characterization of solutions with the desired characteristics.

In the first level, this study addresses the conceptual question of recording and transmission of signal and the choice of good mathematical models for the processing of information and minimization of error inherent in the approaches and in accordance with the principles of the characterized physical devices.

The main work of this thesis is focused on the hierarchical levels of the architecture of the read channel and the integrated circuit implementation of its main block - the filtering block. At the architecture level of the read channel this work presents a comprehensive study on existing methodologies of adaptation and signal recovery of data on magnetic media. This project appears in the sequence of the proposed solution for a low-cost, low consumption, low voltage, low complexity, using CMOS digital technology for the performance of a DFE (Decision Feedback Equalization) based on the equalization of the signal using integrated analog filters in continuous time.

At the project level of implementation of the filtering block and techniques for implementing filters and its building components, it was concluded that the technique based on transconductance circuits and capacitors, also known as *gm-C* filters is the most appropriate for the implementation of very-high-frequency adaptive filters. We defined in this lower level, two sub-levels of depth study for this thesis, namely: research and analysis of optimal structures for the design of state-space filters, and the study of techniques

for the design of transconductance cells in digital CMOS circuits for the implementation of continuous time integrated analog filters.

Following this study, we present and compare two filtering structures operating in the space of states, corresponding to two alternatives for achieving a realization of an adaptive equalizer by the use of a continuous-time third order allpass filter, as part of a read-channel for magnetic media devices.

As a constituent part of these filters, we present a technique for the realization of transconductance circuits and for the implementation of linear capacitors using arrays of MOSFET transistors for signal processing in very-high-frequency integrated circuits using sub-micrometric CMOS technology. We present methods capable of automatic adjustment and compensation for deviation errors in respect to the nominal values of the components inherent to the tolerances of the fabrication process, for which we present the simulation and experimental measurement results obtained.

Also as a result of this study, is the presentation of a circuit that provides a solution for the control of the head positioning on recording/playback systems of data on magnetic media. The proposed block is an adaptive first-order filter, based on the same transconductance circuits and equalization techniques proposed and used in the implementation of the adaptive filter for the equalization of the read channel.

This filter was designed and included in an integrated circuit (Jaguar) used to control the positioning of the read-head done for ATMEL company in Colorado Springs, and part of a commercial product used in removable hard drives fabricated in partnership with a Scottish company.

Keywords: continuous-time adaptive filters, filter structure comparison, signal equalization, standard digital CMOS technology, current-mode signal processing, CMOS transconductors, low consumption, very high frequency, low area, low cost, low complexity.

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List of abbreviations and symbols

ADC ..... Analog to Digital Converter
ATA ..... Advanced Technology Attachment (PATA)
ATAPI ..... Advanced Technology Attachment Packet Interface
BSIM ..... Berkeley Short-channel IGFET Model
CPP ..... Current Perpendicular-to-Plane
CT ..... Continuous-Time
CMOS ..... Complementary Metal-Oxide-Semiconductor
CMRR ..... Common Mode Rejection Ratio
DAC ..... Digital to Analog Converter
DFE ..... Decision Feedback Equalization
DMA ..... Direct memory access
DSP ..... Digital Signal Processor
ESS ..... European Silicon Structures (ES2)
EOT ..... Equivalent Oxide Thickness
EPRML ..... Extended Partial Response Maximum Likelihood
FDTS ..... Fixed Delay Tree Search
ft ..... Transition frequency
gm ..... Transconductance (or transcondutor)
GMR ..... Giant Magnetoresistance
GSRR ..... Ground Supply Rejection Ratio
LMS ..... Least Mean Squares
LPF ..... Low Pass Filter
HDD ..... Hard Disk Drive
IC ..... Integrated Circuit
IDE ..... Integrated Drive Electronics (ATA)
MDFE ..... Multilevel Decision Feedback Equalization
MLSD ..... Maximum-Likelihood Sequence Detector
MOSFET .... Metal-Oxide-Semiconductor Field Effect Transistor

MR ..... Magnetoresistance

NMOS ..... N-type Metal-Oxide-Semiconductor

NCQ ..... Native Command Queuing

OTA ..... Operational Transconductor Amplifier

ISI ..... Intersymbol Interference

IGFET ..... Insulated-Gate Field Effect Transistor

PCB ..... Printed Circuit Board

PCMCIA .... Personal Computer Memory Card International Association

PLL ..... Phase-Locked Loop

PLO ..... Phase-Locked Oscillator

PMOS ..... P-type Metal-Oxide-Semiconductor

PR ..... Partial Response

PR4 ..... Partial Response (class 4)

PRML ..... Partial Response Maximum Likelihood

PSRR ..... Power Supply Rejection Ratio

PTAT ..... Proportional To Absolute Temperature

RAID ..... Redundant Arrays of Inexpensive Disks

RAM-DFE ... RAM-based Decision Feedback Equalization

RLL ..... Run–Length Limitation

SAR ..... Successive Approach Register

SATA ..... Serial ATA

SCSI ..... Small Computer System Interface

SNR ..... Signal Noise Ratio

SSD ..... Solid-State Drive

THD ..... Total Harmonic Distortion

TMR ..... Tunneling Magnetoresistance

UDMA ..... Ultra DMA

UMTS ..... Universal Mobile Telecommunication System

VGA ..... Variable Gain Amplifier

Chapter 1

Introduction

Objectives 3

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1.1 Objectives

The goal of this work is to conceive, design and test a low voltage, low power adaptive continuous time 3rd order allpass equalizer implemented in a 0.5μm standard digital CMOS process, for use in a magnetic disk DFE read channel. The filter has been integrated using a *gm*-C topology for better high frequency performance. An orthonormal-based structure adopted for the sake of adaptability is presented, along with a low-mismatch high bandwidth transconductor. The *gm*s are pseudo-differential balanced transconductors and the integrating capacitors are implemented using polarized transistor arrays consisting of 12.5fF unit size cells. The parasitic input capacitance in the *gm*s is subtracted from the respective integrating capacitors thus allowing the transconductors to work at very high frequency. Automatically tuning the frequency of poles compensates for process tolerances that influence the effective value of the active devices. The proposed system is particularly efficient in the fast growing market of portable computer applications.

1.2 Motivation

The motivation of this work was the search for continuous time filtering solutions for reading in data recording and reproduction systems on magnetic media, with costs and consumption (total size less than 1mm^2 and consumption than 1mW/pole), lower than the circuits available. Accordingly, as was done in this work, the rapid development of microelectronics technology raised very significant efforts worldwide in order to investigate new techniques for implementing such filters in monolithic integrated circuit, especially in CMOS technology (Complementary Metal Oxide Semiconductor). We present a comparative study on different hierarchical levels of the project, which led to the realization and characterization of solutions with the desired characteristics.

In the first level, this study addresses the question of recording and transmission of signal and the choice of good mathematical models for the processing of information and

minimization of error, inherent to the approaches in accordance with the physical principles of the characterized devices.

The work's main thesis is focused on the hierarchical levels of the architecture of the read channel and integrated circuit implementation of its main block - the block of filtering. At the architecture level of the read channel, it presents a comprehensive study on existing methodologies and adaptation of signal recovery of data on magnetic media. This project appears in the proposed solution for a low-cost, low consumption, low voltage, low complexity, based on CMOS digital technology, to implement a DFE (Decision Feedback Equalization) based equalizer of the signal using continuous time integrated analog filters.

At project level of implementation of the filtering block and techniques for implementing its constituents, it was concluded that the technique based on transconductance (*gm*) and capacitors, also known as *gm*-C filters is the most appropriate for achieving adaptive filter in very-high-frequency. In this lower level, two sub-levels of depth of study in this thesis are defined, namely: research and analysis of structures for optimal design of filters using state-space representation, and the study of techniques for implementation in digital CMOS circuits for transconductance for the implementation of integrated analog filters in continuous time. Following this study, we compare two structures of filters in the space of states, corresponding to two alternatives for achieving an adaptive equalizer by a continuous-time third order allpass filter, for use in a channel of reading data on magnetic media.

As a constituent part of these filters, we present a technique for the realization of a transconductance cell and integrating capacitors using linear arrays of MOSFET transistors for signal processing in very-high-frequency integrated circuit using sub micrometric CMOS technology. There are methods capable of automatic adjustment to compensate for the errors against the nominal values of components due to the manufacturing tolerances for which we present the simulation results and experimental measurements obtained.

Also as a result of this study, we designed an adaptive first order filter based on the proposed transconductance cell and using the same equalization techniques. This block

is proposed to control positioning of the head of reading systems in recording/playback data on magnetic media.

1.3 Context and state of the art

The first solutions in magnetic hard disk drives for personal computers were proposed in 1980 closely followed by the first 3 1/2" floppy drives in 1981. Early designs used conventional peak-detection read channels, basically relying on zero crossing of the differential input signal, to sample the input in its local minimum or maximum value. These designs have gradually evolved to present days including equalizer blocks for pulse-slimming and more complex clock recovery schemes.

The main limitation of peak detection read channels is that the data-encoding scheme doesn't allow the use of more aggressive data storage techniques based on the augment of user bit density. This limitation in linear data density strongly compromises the desired storage capacities, whilst maintaining slow data transfer speeds based on single peak detection schemes. As bit density is increased, these analog peaks are processed at higher rates, thus significant overlapping occurs, leading to inter-symbol interference (ISI) and possibly to data bit errors.

In 1990 IBM introduced its first-generation partial-response[1] maximum likelihood (PRML) read channel technology in hard disk-drives [1.1]. The PRML approach differs from traditional peak detector read channels, which do not compensate for ISI, by using advanced digital filtering processing to shape the read signal frequency and timing characteristics to a desired partial response, and by using maximum-likelihood digital data detection to determine the most likely sequence of data bits that was written to the disk. This sequence-detection method is implemented using the Viterbi[2] algorithm for sequence detection [1.2].

[1] Partial Response (PR) coding in magnetic recording was first proposed by Hisashi Kobayashi in 1970.

[2] Andrew Viterbi invented this algorithm in 1967 for decoding convolutionally encoded data.

PRML based read channels use an analog to digital converter to sample the input read head signal and advanced digital signal processing (DSP) to allow higher bit density at faster data rates with improved data integrity. The increase in the amount of allowed ISI is compensated at the cost of complexity, power and silicon area. This is particularly significant and relevant considering the desirable increase in data speed, especially due to the power consumption increase with the operation frequency.

Alternative architecture delivering equivalent performance to the most advanced partial response read channel solutions, were presented [1.3] based on decision feedback equalization (DFE)[3]. The basic DFE architecture consists of two equalizing finite impulse response (FIR) filters and a slicer. The forward equalizer is used for *precursor* ISI cancellation and the backward equalizer is a non-linear *post cursor* ISI remover.

This is the common structure from which derived some of the schemes described in chapter 3, such as fixed-delay tree search decision feedback (FDTS/DF), RAM-based DFE (RAM-DFE)[4] and multilevel decision feedback equalization[5] [1.5] (MDFE).

In August 1996, Philips Semiconductors announced its first standard RAM-DFE read channel device [1.6], a fully-adapted self-training DFE scheme compatible with a wide range of read head and media interfaces. Adaptation allows improved bit-error rate (BER) achieving signal-to-noise ratio equivalent to PR4 read channel, at increased user data bit density.

Considerable effort was employed in the developing of a low power continuous time adaptive forward equalizer alternative to the FIR approach usually used with DFE.

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[3] Decision Feedback Equalization (DFE) was first presented in 1967, by M. Austin as an equalizing technique for dispersive channels. Adaption capability was further proposed and added to the system in 1970 by D. George *et al.*, but it was only in 1996 that this scheme was firstly integrated in a commercial circuit as a practical alternative to peak detection techniques

[4] The first DFE equalizer using RAM-Based equalization [1.4] was published in 1989 by Fisher *et al.*

[5] Multilevel Decision Feedback Equalization (MDFE) was first presented in 1993, by J. Kenney as an equalizing technique for dispersive channels as an efficient realization of FDTS/DF.

In February 1995, Professors José Epifânio da Franca and John Kenney proposed the development of a continuous-time filter solution for the realization of the forward equalizer as the starting problem to be addressed by the work developed in this thesis. This work was carried out at the integrated circuits and systems group in IST until 2000 and later on completed and written under the supervision of professors Augusto Albuquerque and Francisco Cercas at ISCTE.

The following tables summarize the most relevant publications in the implementation of PRML read channels and the main characteristics in terms of technology, data rate, power and area of the equalizer solutions presented. Table 1.1 shows the characteristics of available equalizers and Table 1.2 the total area and power consumption of PRML solutions.

Table 1.1 – Equalizer evolution.

Year	Technology	Freq./Data rate	Power	Area
1993	1.0μm CMOS	7.1 MHz	988 mW	146 mm^2
1993	2.0μm CMOS	40 MHz	500 mW	31 mm^2
1994	1.2μm CMOS	100 MHz	900 mW	44 mm^2
1995	0.8μm CMOS	240 MHz	426 mW	2.9 mm^2
1995	0.5μm BiCMOS	250 MHz	340 mW	1.8 mm^2
1996	0.6μm CMOS	200 MHz	507 mW	13 mm^2
1996	1.0μm CMOS	160 MHz	460 mW	23 mm^2
1997	0.6μm CMOS	150 Mb/s	90 mW	0.8 mm^2
1998	0.25μm CMOS	360 Mb/s	21 mW	-
1999	1.0μm CMOS	80 Mb/s	280 mW	6.7 mm^2
2002	0.5μm CMOS	100 Mb/s	130 mW	1.3 mm^2
2005	0.18μm CMOS	70 MHz	21.8 mW	-
2007	0.18μm CMOS	160 MHz	15 mW	-
2008	0.18μm CMOS	400 MHz	80 mW	-

Table 1.2 – PRML channel evolution.

Year	Technology.	Data Rate	Power	Area
1994	0.8μm BiCMOS	64 Mb/s	2.85 W	-
1994	1.0μm BiCMOS	72 Mb/s	0.78 W	-
1994	0.8μm CMOS	36 MHz	0.69 W	51 mm^2
1995	0.5μm BiCMOS	16 MB/s	1.20 W	26 mm^2
1996	0.6μm CMOS	130 Mb/s	1.35 W	28 mm^2
1996	0.7μm BiCMOS	150 Mb/s	1.55 W	47 mm^2
1996	0.5μm BiCMOS	200 Mb/s	0.85 W	20 mm^2
1999	0.35μm CMOS	300 MHz	0.23 W	0.8 mm^2
2001	0.18μm CMOS	150 Mb/s	0.18 W	1 mm^2
2006	0.35μm CMOS	300 MHz	-	12.8 mm^2

1.4 Layout of the thesis

The first chapter of the thesis introduces the subject of study, its overall motivation and the objectives pursued during this work. It also describes the structure of the document and statement of originality of the proposed solutions.

The second chapter of this thesis is a brief characterization of the physical elements involved in the magnetic disk storage process. The basic theoretical definitions and models of the read channel are introduced. The read and write processes in magnetic storage are explained together with the definition of simple key concepts such as user bit density and intersymbol interference. The building blocks of disk drive electronics are identified and succinctly described. A general analysis of magnetic disk drive products available on the market is summarized in terms of expectable evolution in main characteristics of the device.

The third chapter introduces the existing coding algorithms involved in the storage and readback process of magnetically stored information and the basic read channel architectures. Run length limitation and its advantages in band limited communication channels is explained. The principal read channel architectures are described and compared in terms of performance. Partial Response and Multilevel Decision Feedback Equalization (MDFE) read channel architectures are introduced.

The forth chapter presents two practical solutions for the forward equalizer in MDFEs architecture, the critical block of the system. Recursive continuous-time adaptive filters are proposed for the implementation of equalizers for magnetic disk drive read channels. A canonical structure and an orthonormal structure recursive filter are proposed and compared at transistor level. Tuning schemes and LMS algorithms are analyzed.

The fifth chapter introduces the building blocks of the proposed circuits. A self-biased transconductance cell is presented for the implementation of very high frequency current mode *gm*-C filters. The influence of short channel effects is analyzed. The use of biased MOSFET capacitor arrays in standard digital CMOS technology is studied.

Chapter six describes the experimental procedure and results of the proposed integrated circuits. Firstly it presents a continuous time servo burst demodulator for magnetic disk drives based on the building blocks introduced in chapter five. Secondly it presents simulation and measurement results of the continuous time equalizers and of the transconductor cell proposed.

The seventh and final chapter summarizes the conclusions of this thesis and presents some suggestions for further research and development.

1.5 Original contributions

The original contributions of this thesis are:

- Development of a fully analog continuous-time integrated equalizer for the implementation of a multi-level decision feedback equalization (MDFE) read channel [1.7] (Chapter 5).

- Proposal and development of an orthonormal state-space current-mode filter for the implementation of a continuous-time third order adaptive equalizer for MDFE [1.7] (Chapter 5).
- Comparison of orthonormal and canonical filter structures based on the physical limitations at circuit-level design with simulated and measured results [1.7] (Chapter 5).
- Development of an auto-biased 0.5μm CMOS transconductor cell for the implementation of very high frequency current-mode *gm*-C filters [1.8] (Chapter 4).
- Proposal and development of a first order filter for servo-burst demodulation in magnetic read channels [1.9] (Chapter 6).
- Comparison of different design approaches to equalization in hard disk read channels [1.10].

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Chapter 2

The recording and readback processes

Nonvolatile memory storage devices 15
Physical aspects of the hard disk 16
Playback process 19
Write process 24
Read back channel model 35
Disk-drive electronics 42
Market trends and evolution 45
Conclusions 48

2.1 Introduction

This chapter describes the physical elements and principals involved in the magnetic disk storage process. The basic theoretical definitions and models of the read channel are introduced. The read and write processes are explained together with the definition of simple concepts such as user bit density and intersymbolic interference. The building blocks of disk drive electronics are identified and succinctly specified. A general analysis of magnetic disk drive products available on the market is summarized in terms of expectable evolution in the main characteristics of the device.

2.2 Nonvolatile memory storage devices

Nonvolatile memory devices are crucial to complex systems allowing information to be safely and persistently stored in the absence of power consumption. This is relevant either for massive storage systems as well as for mid-sized systems requiring little more than start-up code storage.

The first solutions for nonvolatile memory come from the fifties with magnetic tape drives in mainframe computers. Slow head positioning and sequential access where strong limitations for this early devices. Magnetic hard drives and floppy drives where proposed in 1981 providing fast head positioning on disk and hence low access time to stored data. In a hard disk drive (HDD) the non-volatile storage is accomplished through digitally storing the data on rapidly spinning platters with a magnetic surface platter. This is a circular disc which has a magnetic surface that stores the data. The first HDDs had multiple platters usually made of aluminum with a thin film carbon coating applied to each side.

E2PROM and Flashrom, where originally used to keep a copy of firmware images such as BIOS. More recently, in 2011, solid-state drive (SSD) have reached the market of nonvolatile data storage for personal computers. These devices use integrated circuit memory to store data persistently and electronic interfaces compatible with traditional block input/output interface of traditional hard disk drives. Since SSDs have no moving mechanical components, the access time is extremely low, and power consumption is also low when compared to HDD. The stored bits are safer in a SSD and the device is more

robust than a conventional HDD. For these reasons, some predict that in time SSD may overtake HDD as the preferred nonvolatile media. Nevertheless, the low price per TB for the HDD devices, is much lower than that of SSD devices, making HDD a growing market for years to come.

2.3 Physical aspects of the hard disk

Magnetic support has long been the prime choice for non-volatile data storage. More particularly, magnetic disk drives have taken an increasingly greater share of these tasks. The physical characteristics of magnetic disk devices are a fine match for the requirements of swift and non-sequential recording and playback of digitally stored data. Unlike their magnetic storage predecessors, magnetic disk drives have rapidly evolved to combine: mass storage capability, fast sequential access and long-term reliability akin to magnetic tape devices; with the inexpensive, flexible and efficient non-sequential access of floppy-disk drives. Moreover, the widespread use of this device has rapidly pushed its performance way beyond these magnetic storage counterparts in all relevant parameters. These wide range high performance uniqueness meet in a fine compromise, that allow its use as a virtual random access memory expander as efficient as its use in the hosting of massive long-standing secure data banks.

Although some still proudly preserve some amazing prototypes of huge size aluminum disks used during the early ages of magnetic disk storage, mass production of desktop computer magnetic disks quickly matured to fit in 3 ½" bays. With the advent of portable computers, regular pushes towards slender and lighter laptop equipment have further forced magnetic disk devices from 3.5" to 2.5", 1.8" or even 1.3". Recent market available applications present a complete 0.85" disk-drive solution of traditional architecture scaled to fit a thumbnail, defying the obvious appeal of massive non-volatile *Flash* memories.

Regardless of its size, the basic physical components of a magnetic disk storage apparatus are depicted in Fig. 2.1.

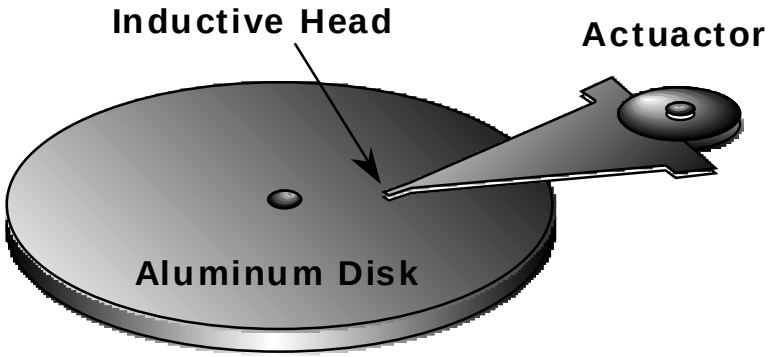

Fig. 2.1 – Physical components of a magnetic disk drive storage system.

A magnetic disk device mainly consists of four basic physical components:

- One or several **aluminum disks**, each providing an endurable physical foothold for the thin magnetic film coating that contains all the information stored on the disk.
- The **head actuator** or servo actuator that is responsible for the positioning[6] of the magnetic head in a random track on the disk.
- The **read head**[7] at the end of the actuator arm floats merely nanometers[8] over the magnetic film coating, and caries out the sensing and imposing of the magnetic fields from and onto the media as the disk data is read or written.
- The **spindle motor** is used to steer the movement of the disk(s), spinning its angular velocity up to 10000 revolutions per minute (rpm). This motor is accountable for about 40% of the total disk drive power.

[6] This time is usually defined as *access time*, and is one of the main characteristics of the disk along with total capacity and data transfer rate.

[7] Usually made of high permeability alloy to improve flux sensibility.

[8] The mechanical principals and physical dimensions are akin to other magnetic storage systems such as digital videotape recorder or VHS.

The magnetic film surface veneers, with approximately two thousand circular concentric tracks[9] per centimeter, contain all the information on tiny independently oriented magnets. These slight magnetic records are packed at approximately 40000 bits per centimeter yielding out binary encoded data.

The magnetic tracks on the media surface are narrow concentric rows of very small magnets containing user information. These magnets can have one of two possible orientations: *clockwise(left)* or *anti-clockwise(right)* — see Fig. 2.2 — such that a transition from left to right (or right to left) in the magnetic orientation induces a voltage across the coil proportional to the flux variation with time, as given by Faraday's law of induction, represented in equation (2.4).

The user bit[10] is recorded on the disk surface driven by a magnetic flux throughput imposed on the magnetic head during the write process. Once stored, the bit can be sensed during playback as a very low amplitude[11] voltage pulse that is subsequently processed and transmitted by the read circuitry back to the data bus via the host interface controller.

Fig. 2.2 shows the data flux between the disk media and the read/write circuitry. The electronic front-end is usually a dedicated pre-amplifier integrated circuit physically placed close to the head, with large bandwidth and low noise specifications used for gain boosting of these low voltage pulses. This IC separates the signal path into two split differential data channels, one for writing and one for reading. Both continuous time differential signals are analog interfaces between the read/write channels and the front-end electronic blocks involved in the magnetic storage and read back processes.

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[9] The tracks are further divided in angle defined portions (like pie cuts) called sectors, each having 512 bytes of user data preceded by a header containing servo fields for correct track positioning and monitoring, and by preambles that assist in gain setting and clock recovery.

[10] Logical 1 if there is a transition on flux magnetization (either *left to right* or *right to left*) and logical 0 if no transition occurs.

[11] The raw output pulses induced on the read head have approximately 1mV peak to peak (ptp).

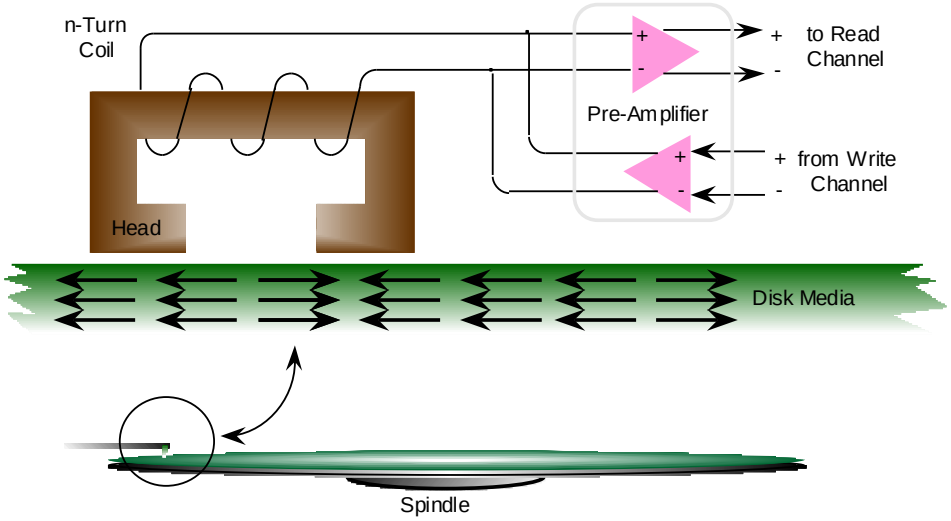

Fig. 2.2 – Data flux between the disk media and the read and write circuitry.

2.4 Playback process

The playback process starts when the host interface controller receives a read order from the host processor. The command is usually originally initiated by the CPU and is issued onto the disk electronic blocks through a SCSI[12] or IDE[13] bus controller IC. The host interface controller forwards the order to the servo controller, which in turn positions the head actuator onto the designated track, according to the track ID stored on the servo sectors. Once the head is in a fixed position, the rotating movement of the disk allows that the read channel IC can correctly access and feedback the stored user data to the host interface controller. The worst-case elapsed time between data request and data ready at the bus is defined as the access time of the disk. Due to the involved complexity and

[12] Small Computer System Interface is a high-speed parallel interface standard defined by the American National Standards Institute (ANSI) used for connecting microcomputers to peripheral devices.

[13] Integrated Device Electronics is one of the most widespread disk-drive interface, in which the controller electronics reside on the drive itself, eliminating the need for a separate adapter card and offering advantages such as look-ahead caching.

physical constraints this access time is usually in the order of 10 to 20 milliseconds. Naturally this significant delay overhead is negligible in the general case of sequential disk access to large data blocks. Moreover, in most cases, the host interface controller buffers the read data in local memory blocks[14], before being transferred back to the host processor. This is usually combined with sophisticated software disk caching schemes.

Therefore, the fundamental electrical characteristic of the disk is the user data transfer rate. Unfortunately, high transfer rates imply costly consumption requirements[15], and hence, especially in the case of portable systems, the power consumption takes the major role in the achievable balance between speed and battery operation autonomy.

Inductive head

The inductive head hovers over the surface of the disk, at the end of the actuator arm. The traditional inductive head is a C-shaped highly permeable microscopic magneto-sensitive alloy embraced by a coiled wire similar to those of ferrite read heads in tape recorders. A wired coil can be used for both reading and writing of bits to the disk surface. By imposing a strong magnetic field in the gap of the C, and thus on the recording surface adjacent to the gap the media can be magnetized. To read a magnetized stored bit, the head generates a current in the coil, when the media rotates past the head core it generating a voltage drop on the wire. In HDD the field is very strong and the gap is quite narrow, determining the minimum size of a recorded bit, and hence, the linear and areal density.

The relative movement of the stored magnets on the disk's surface in respect to the read head causes a variation of the magnetic flux that flows through the head core. The variation in time of the magnetic flux density flow through an electric circuit wire loop generates an electric field, as results from Faraday's law expressed in its integral form by

[14] See the electric block diagram in Fig. 2.16 on page 42.

[15] Note that the power consumption in digital blocks is roughly proportional to the signal frequency, and hence to the data transfer rate.

$$\oint_C \vec{E} \cdot d\vec{l} = -\frac{\partial}{\partial t}\left(\iint_S \vec{B} \cdot \vec{N}\, ds \right) \tag{2.1}$$

where *S* represents any surface delimited by the oriented closed path wire contour here denoted as *C*. Vector $\vec{B}$ denotes the magnetic flux density and $\vec{N}$ is a unitary vector perpendicular to surface *S*.

The read circuit depicted in Fig. 2.2 can be treated as a simple wire loop with a resistive load, immersed in a time varying magnetic field[16], and therefore the potential difference at the edges of the load is given by the following line integral

$$V(t) = \oint_C \vec{E} \cdot d\vec{l}\ . \tag{2.2}$$

Using the definition of magnetic flux

$$\phi = \iint_S \vec{B} \cdot \vec{N}\, dS \tag{2.3}$$

and combining it with equations (2.1) and (2.2) indicates that the variation of the magnetic flux, flowing through an electric circuit generates a voltage at the wire terminals. This is one of the basic principles of electromagnetic induction as was first stated by Faraday in 1831, and can be expressed in a simplified form by equation (2.4) known as Faraday's law of induction

$$V(t) = -\frac{d\phi}{dt}\,. \tag{2.4}$$

The polarity of the induced voltage and the direction of the electric field through the wire, produce a current flow on the circuit that opposes the change of magnetic flux, as follows from Lenz's law. The minus signal on equations (2.1) and (2.4) denotes this statement.

[16] Time varying fields are non-conservative, hence conservation of energy does not apply.

This also derives from Maxwell's treatise on electricity and magnetism published in 1873 — closely based on Faraday's work — on equation (2.5) that expresses the law of induction in its differential form

$$\vec{\nabla} \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}. \tag{2.5}$$

This is comprehensible from the application of Stoke's theorem to the line integral of the electric field $\vec{E}$ as depicted in (2.6), which yields equation (2.1).

$$\oint_C \vec{E} \cdot d\vec{l} = \iint_S \vec{\nabla} \times \vec{E} \cdot \vec{N}\, ds = \iint_S -\frac{d\vec{B}}{dt} \cdot \vec{N}\, ds \tag{2.6}$$

Therefore, the inductive head effectively implements a magnetic flux intermediate to access the user data stored on the disk surface. Multiple coils of the circuit wire are usually used to embrace the inductive head, hence the effective surface of the *n*-turn delimited solenoidal path is equivalent to *n* times the surface of a single wire loop. This increases the signal strength during the read process, whilst reducing the current necessary to generate the desired combined conducted magnetic field during the write process.

As a result equation (2.4) is in this case expressed by equation (2.7)

$$V(t) = -n\frac{d\phi}{dt}. \tag{2.7}$$

Consequently, any transition in the magnetic field flowing through the head induces a voltage across the wire proportional to flux variation with time and to the number of coiled turns.

The read and write principals of the inductive head did not change with Metal-in-gap (MIG) or thin-film heads (TFH). In MIG read heads the properties of soft alloys like permalloy (NiFe) improve magnetization saturation, allowing twice the magnetic field. TFH are made using photolithography similar to semiconductor technology, allowing even higher read and write accuracy.

Magnetoresistance (MR) and giant magnetoresistance (GMR)

An improvement was to create a separate head using the magnetoresistive (MR) effect which changes the resistance of a material in the presence of magnetic field. MR heads are able to read very small magnetic features reliably, but cannot be used to create the strong field used for writing. The term AMR (A=anisotropic) is used to distinguish it from the later introduced improvement in MR technology called GMR (giant magnetoresistance). The introduction of the AMR head in 1996 by IBM led to a period of rapid areal density increases of about 100% per year. In 2000 GMR, giant magnetoresistive, heads started to replace AMR read heads.

Tunneling magnetoresistive (TMR)

In 2005, Seagate introduced the first drives to use tunneling MR (TMR) that can be activated before starting the write operation, hence ensuring that the head's write field fully saturates the magnetic disk medium. This improves the written magnetic transitions and decreases the separation to the disk medium for improved signal strength.

Perpendicular magnetic recording (PMR)

An important advance was the transition to perpendicular magnetic recording (PMR). The main difference being that the write flux is driven perpendicularly to the media as opposed to in parallel to the media. This has implications on the write head format and on the disk media since it implies the use of an additional soft magnetic under layer, serving to augment field strength written to the disk media as shown in Fig. 2.3. The packing of the flux transaction has improved areal density and speed potential.

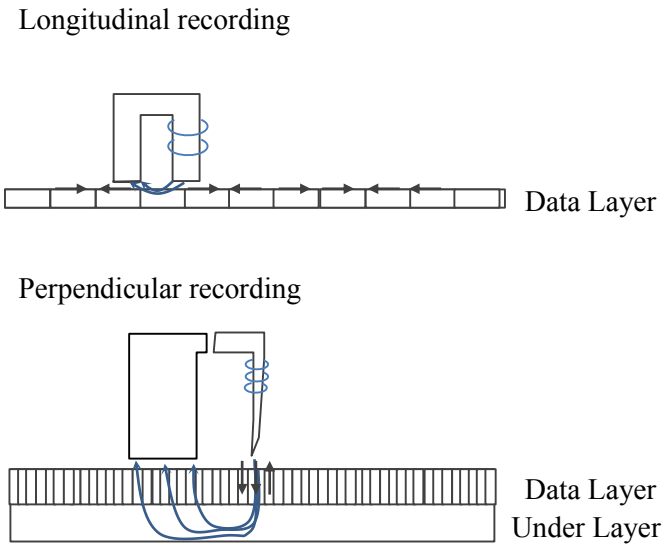

Fig. 2.3 – Perpendicular to disk magnetic recording.

2.5 Write process

The write process is also triggered when the host interface controller receives an order from the host processor, commanding that a given data sequence is stored onto the disk. Typically, some or all of the data will be transferred in advance, packed into blocks and buffered locally. As described for the read process, the servo controller has to position the head actuator onto a designated track. Once the head is in position, the write bits are forwarded to the write channel and are output to the magnetic head, through which they are forced onto the rotating disk. The physical constrains determining the access time during a write procedure are similar to the referred for the playback process. Although the host interface bus and magnetic head are shared for both write and read commands, the write channel and magnetic recording fundamentals justify additional analysis.

Inductive head

The basic principal behind non-volatile recording of a bit on the surface of a magnetic disk is the establishment of a magnetic field imposed by an electric current flow

through an electric wire. The fundamental law relating magnetic field strength and electric currents was ascertained in 1820 by Biot and Savart, and is expressed in its differential form by equation (2.8), the well-known Biot-Savart law

$$d\vec{H} = \frac{I\, d\vec{l} \times \vec{u}_r}{4\pi r^2} \tag{2.8}$$

where $d\vec{H}$ denotes the differential magnetic field strength, for a given position of which r and $\vec{u}_r$ are the distance and unit vector respectively. Distance r and vector $\vec{u}_r$ are referred to an infinitesimal current element denoted as $I\, d\vec{l}$.

Therefore, the magnetic field strength vector $\vec{H}$ induced on any position in a tri-dimensional space by an electric circuit can be obtained by integrating the influence of all current elements in respect to that point. Hence, this yields equation (2.9), where C denotes the closed circuit path and is valid for any chosen physical geometry.

$$\vec{H} = \frac{1}{4\pi} \oint_C \frac{I\, d\vec{l} \times \vec{u}_r}{r^2}. \tag{2.9}$$

A simple inference is that a stationary current, i.e. a constant velocity charge flow, through an electric wire generates a static magnetic field. This basic concept plays an important role in saturation recording[17].

The magnetic field denoted by $\vec{H}$ is non-conservative, this is patent in Ampere's law, given by

$$I = \oint_C \vec{H} \cdot d\vec{l} \tag{2.10}$$

where C is a closed oriented path and I is the enclosed current.

The differential form of this law combined with the displacement current density $\frac{d\vec{D}}{dt}$ term — introduced by Maxwell's work — added to the current density vector $\vec{J}$

[17] See page 30 for an extend description of saturation recording.

yield the curl of the magnetic field, as given by (2.11), the unifying equation between non-stationary electrical and magnetic fields

$$\vec{\nabla} \times \vec{H} = \vec{J} + \frac{d\vec{D}}{dt}. \tag{2.11}$$

Vector $\vec{D}$ represents the electric flux density vector and is independent of the permittivity[18] of the medium. The definition of electric flux density can be more easily understood together with Gauss's law in its integral form

$$\oiint_S \vec{D} \cdot d\vec{S} = \iiint_V \vec{\nabla} \cdot \vec{D} \; dV = \iiint_V \rho \; dV = Q \tag{2.12}$$

where ρ represents the charge density in volume V bounded by a closed surface S, and Q is the enclosed electric charge. The differential form of Gauss's law represents the same physical principal in a condensed format and is given by the following equation

$$\vec{\nabla} \cdot \vec{D} = \rho \,. \tag{2.13}$$

An analogous principal is valid when the charge density inside a closed surface varies in time. The intuitive fact that the flux of current density to the outside of a closed surface S is symmetrical to the variation of charge in its interior is expressed in its integral form by the following equation, commonly known as the continuity equation

$$\oiint_S \vec{J} \cdot \vec{N} \, dS = \iiint_V \vec{\nabla} \cdot \vec{J} \, dV = -\iiint_V \frac{\partial \rho}{\partial t} dV \,. \tag{2.14}$$

Note that the current density vector $\vec{J}$, given by the definition of current density for a generic surface S

$$I = \iint_S \vec{J} \cdot \vec{N} \, dS \,, \tag{2.15}$$

[18] The electric flux density is proportional to electric field strength $\vec{E}$ according to the permittivity of the medium as given by $\vec{D} = \varepsilon \vec{E}$.

represents the summed contribution of conduction and convection currents, resulting from the movement of charge densities under the influence of an electrical field respectively in a conducting or non-conducting region. The continuity equation (2.14) relating current and charge can be more easily expressed in its differential form by

$$\vec{\nabla} \cdot \vec{J} = -\frac{d\rho}{dt} \tag{2.16}$$

where ρ represents charge density.

However, it is generally used in its integral form representing the current flowing through an open crossed-sectional area as derives from equations (2.14) and (2.15), which defines current flow in the direction of the current density vector $\vec{J}$, as the rate at which electric charge q passes through this area, and is expressed by the following equation

$$I = \frac{dq}{dt}. \tag{2.17}$$

The forcing of a current flow on the wire coiled around the magnetic head generates a magnetic field.

The superimposition of the magnetic fields generated by various contiguous wire loops naturally tends to augment the inner magnetic field and cancel out outer and non-normal components, as shown in Fig. 2.4.

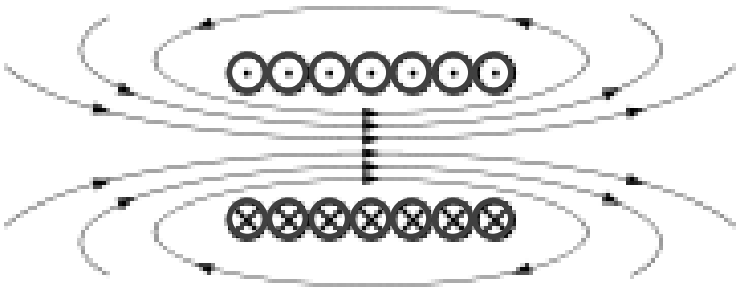

Fig. 2.4 – Magnetic flux generated by a *n*-turn.

This practical choice allows a good control of magnetic flux even in the absence of high permeability media. Besides inductive heads, this is also a commonly used geometry[19] in transformers, inductors, antennas, etc…

Considering this a good approximation we can assume that the magnetic flux is proportional to the write current as given by

$$\phi = L \cdot I \tag{2.18}$$

Using the common ideal inductor model approximation, equation (2.18) can be expressed by the following equation, where n is the number of coiled turns; l and S respectively designate the effective length and section of the magnetic head; and μ denotes the permeability of the read head material.

$$\phi = \mu \cdot \frac{n^2 \cdot S}{l} \cdot I \tag{2.19}$$

Considering magnetic flux definition given by equation (2.20), where $\vec{B}$ is the magnetic flux density vector and $\vec{N}$ is a unitary vector perpendicular to surface S.

$$\phi = \iint_S \vec{B} \cdot \vec{N} \, dS \tag{2.20}$$

Naturally, as results from Maxwell's well-known equation

$$\vec{\nabla} \cdot \vec{B} = 0 \tag{2.21}$$

the divergence of the magnetic field density vector is zero, consequently there are no physical magnetic charge sources and therefore the result of the integral in equation (2.20) is zero for whatever selected closed surface S. This also results from the application of the divergence theorem to equation (2.22), where V denotes the volume enclosed by surface S.

[19] The perimeter of the wire section should be much less than signal wavelength.

$$\iint_S \vec{B} \cdot \vec{N}\, dS = \iiint_V \vec{\nabla} \cdot \vec{B}\, dV = 0 \qquad (2.22)$$

Nevertheless, when applied to a non-closed surface, a non-zero value results from the definition of magnetic flux. Naturally, a symmetrical value is obtained when considering any surface with the same contour and opposite orientation, since together they form a closed surface and therefore equation (2.22) applies.

Likewise, a magnetic flux is driven out of one of the edges of the head slit and returns through the other edge closing the magnetic field lines, again in accordance with equation (2.21). Logically the magnetic flux will follow the less magnetically reluctant medium, and since the disk surface coat comprises ferromagnetic material, the highest permeability path is through the disk plane, as shown in Fig. 2.5. To ensure that the magnetic flux traverses the gap to the disk and back to the magnetic head, the size of the head slit must be much greater than the gap between the head and the disk surface. This justifies the extremely low distance between the head and the disk surface. Typical physical dimensions for this gap in the range of 0.1μm to 0.2μm are common in various magnetic recording systems including magnetic tape devices. These physical constrains together with the thrust for slimmer pulses determine the dimensions of the head and justify their fabrication process[20]. Once the magnetic field is forced on to and through the disk surface, it will be enduringly stored as magnetically oriented magnets with negative or positive polarity depending on the stored bit.

[20] Usually carried out in micrometer technology wafer design similar to regular CMOS fabrication.

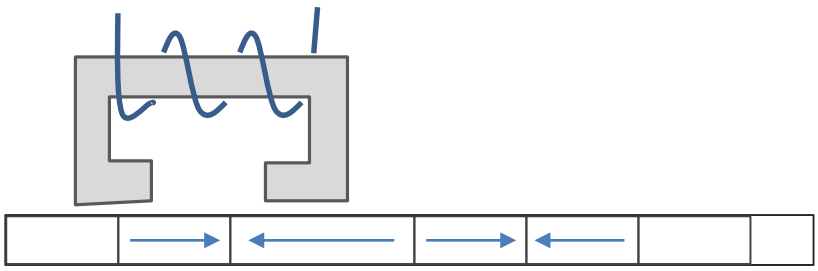

Fig. 2.5 – Interaction between the magnetic head and the disk surface during the saturation recording procedure.

Equation (2.23) defines the magnetic field vector in respect to the magnetic flux density. Note that the magnetic field vector denoted by $\vec{H}$ is independent of the medium, whilst the magnetic flux density is its scaled version according to constant μ, which denotes the permeability of the medium.

$$\vec{B} = \mu \vec{H} \tag{2.23}$$

Neglecting the contribution of border effects depicted in Fig. 2.5 equation (2.20) can be simplified to the following equation

$$\phi = \| \vec{B} \| S \,. \tag{2.24}$$

Saturation recording

In saturation recording the value of the write current has a maximum value and the read head has a magnetization saturation. When the hard disk head passes from over a reversal in the polarization of the media, a small voltage pulse is produced that can be picked up by the detection circuitry. As disk density increases, the strength of each individual magnetic field decreases, hence data must be based on flux reversals, and not the contents of the individual fields.

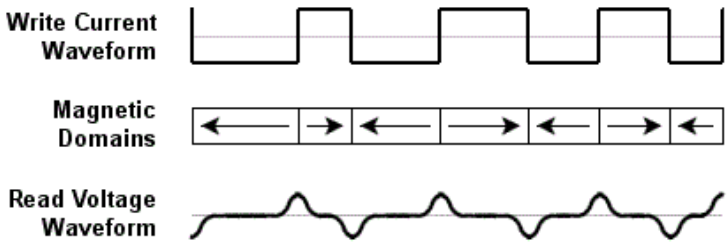

Fig. 2.6 – Interaction between the magnetic head and the disk surface during the saturation recording procedure.

The two basic immediate consequences of this approach are that consecutive ones or zeros may cause read errors to occur. If two consecutive transitions occur the voltage pulses will interfere, especially at high density rates. On the other hand, if no transition in the magnetic polarity occurs for a long period of time, synchronization may be lost and precise determination of the pulse width of an individual pulse will limit the maximum number of consecutive non-transitions on the magnetic media.

A common approach is to code flux changes as ones, and use run length limitation (RLL) with constrains (d, k) imposing that transitions between different symbols occur at least $d+1$ apart from each other and that a transition between different symbols occurs at most k symbols after the previous one.

Aligning too many polarization magnetic fields in the same direction near each other would create a large magnetic field. This is also a reason to encode using flux reversals, combined with run length limitation to keep the number of consecutive fields of same polarity to a minimum. Saturation recording hard disk drives mostly use RLL (1,7) or (2,7).

The write process illustrated in Fig. 2.2 is usually performed through saturation recording. This consists on driving rectangular shaped current pulses through the inductive head[21] using a two level write current. Fig. 2.7 represents an example of the write

[21] Similar analyses can be made for magneto-resistive read heads.

current *I(t)* storing a bit sequence at a frequency of $f=1/T$ using RLL (1,7) coding. Therefore, *T* denotes the elapsed time between consecutive bits and is usually designated as bit period or bit interval.

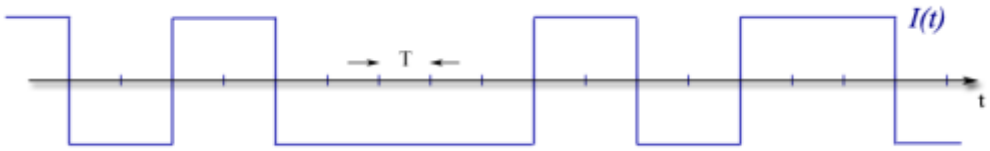

Fig. 2.7 – Write current in saturation recording.

According to the value of the bit that is being recorded to the disk and to the coding scheme, the polarity of the write current causes the steering of the flux either in the direction of disk spin or in the opposite direction. This leads to an inherently bipolar based coding and typically consists of NRZI coding[22]. The penetrating incidence of the flux on the disk surface magnetically stores the bit as a clockwise or anti-clockwise oriented non-volatile pulse.

Equations (2.19) and (2.24) imply that the magnetic flux and magnetic induction field are proportional to the write current. However, the consequent ideal vertical transitions of the magnetic field polarity are not attainable. A more realistic model is to consider finite fall and rise times; hence, in a first order approximation we can consider these pulses as trapezoidal[23] instead of rectangular as depicted in Fig. 2.8. This picture represents the inward and outward magnetic field at the head edges as a function of time.

[22] See page 56 for a description of NRZI coding.

[23] Consult page 149 of reference [2.1]

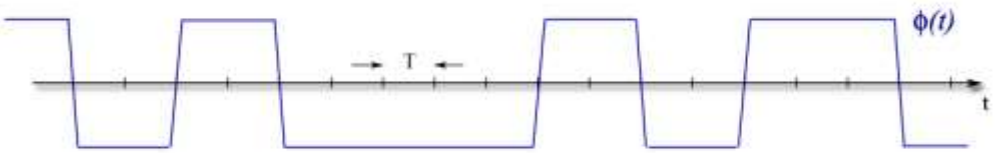

Fig. 2.8 – Stored magnetic flux in saturation recording.

Analyzing more closely the storing of the bit sequence on the surface of the disk, we can assume as a valid local approximation to estimate magnetic induction field linear distribution for the given data sequence, that the spindle drives the disk at a constant linear velocity v_{linear}. This linear velocity is the relative velocity of a fixed stored bit on the disk surface to the read head, which narrowly matches the tangent velocity for that particular track. Hence, v_{linear} is given by the disk spin radian frequency ω_{spin} and by the radius of the track denoted as r, as shown in (2.25). Therefore, the physical distance between adjacent bits denoted by W can be derived by the following equation.

$$W = v_{linear} \cdot T = \omega_{spin} \cdot r \cdot T \tag{2.25}$$

Combing equations (2.20) and (2.25) we can assume that the magnetic flux density forced on to the disk surface, will be enduringly stored as magnetically oriented magnets as can be approximately represented by Fig. 2.9.

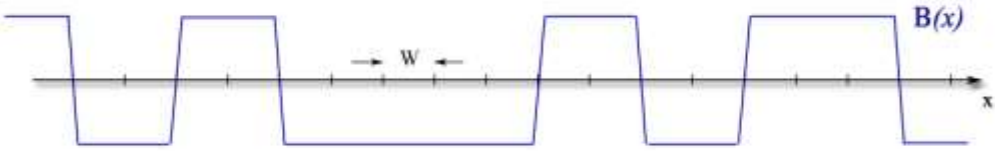

Fig. 2.9 – Stored magnetic induction in saturation recording.

Write precoder

If we know the channel characteristics, part of the equalization task can be performed at the transmitter by precoding the data symbols. This can be used to reduce channel distortion and avoid error propagation. A commonly used precoder polynomial is

$$P(D) = \frac{1}{1 \oplus D^2} \tag{2.26}$$

Write pre-compensation

For enhanced behavior some systems include a non-linear distortion at the beginning of the current pulse during the write process. This is meant to increase the initial slope of the stored pulse, thus accounting for a significant reduction of non-causal intersymbol interference. This technique is denominated as write pre-compensation. The displacement of signal power from the beginning of the pulse to the pulse center and pulse tail slightly increases causal intersymbol interference that is in term compensated using appropriate filtering. This considerably alters the pulse shape depicted in Fig. 2.11, causing it to closely resemble the shape represented in Fig. 2.10.

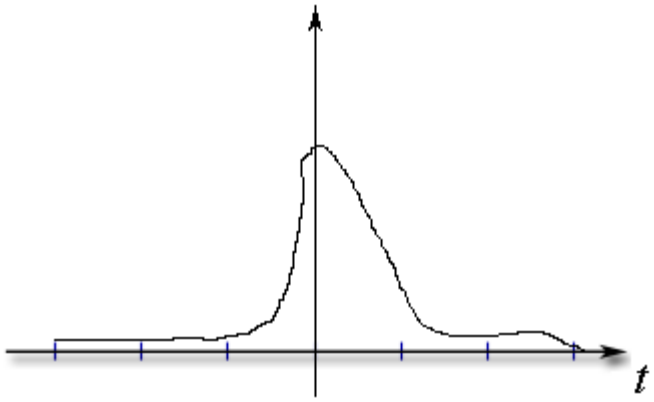

Fig. 2.10 – Write pre-compensated pulse shape.

Various read-channel systems have successfully used this technique to increase bit-packing density and hence augment disk volume and data-rate. Alternatively, or cumulatively, some more sophisticated schemes efficiently allow and compensate the non-causal intersymbolic interference based on the expectable (measured) characteristics of the stored pulse. The pre-cursor non-causal portion of the write/read head response can also

be modeled as a set of poles on the right side of the complex plane in the Argand representation. These can be cancelled by making them coincide with transmission zeros in the read path as is thoroughly described in Chapter 5 .

2.6 Read back channel model

The magnetic head used during the write procedure carries out the read back process. The proximity of the head to the recorded magnets on the disk surface makes it sensible to the flux transitions recorded on the disk. The presence of the magnetic head over the magnets closes the flux path, thus inducing a voltage signal on the coil. According to equation (2.7) this voltage pulse is proportional to the flux variation, therefore a positive voltage pulse is generated when a transition from clockwise to anti-clockwise polarity occurs, and a negative voltage pulse is generated when the polarity of adjacent magnets changes from anti-clockwise to clockwise (or vice versa depending on direction convention). Hence, no impulse is generated whilst polarity is maintained.

The read back procedure and its inherent properties can be treated as any other general purpose communication system. In fact, as will be shown further on, various useful concepts have been adopted from similar theoretical foundations brought from different applications such as cable and line modems. The properties of this communication channel, including read head characteristics and the physical ground rules of the read/write process can be treated as reasonably linear and time invariant. Therefore, a proper linear time-invariant system can be used to model the physical medium of the channel. The step response of the read back procedure is easy to extract based upon measured data from a specific physical medium to a stored positive transition, i.e. a specific head and media can be fully characterized from the analysis of a single flux transition.

Bit density

Conventional magnetic disk storage systems including those based on peak-detect read channel architectures have persistently been forced to decrease the distance between consecutive bits, also referred to as bit interval. Up to a certain level, this allows the increase of disk storage capacity and data transfer rate. However, this thrust towards higher bit density provokes higher non-negligible superimposition of adjacent bits, along with

arduous challenges in terms of clock recovery and higher frequency filtering. The disturbing interference resulting from the overcrowding of neighboring bits is commonly designated as Intersymbol Interference (ISI) and results in significant signal-to-noise ratio (SNR) degradation. This reduction in SNR derives from the decrease and shifting[24] of the peak values of the read head sensed voltage. The effects of intersymbol interference are particularly noticeable when the pulse width is larger than the bit interval, i.e. when the bit density exceeds one.

Naturally, the pulse width should be as small as possible given that thin pulses increase the amount of disk storage capability for a given disk area, and indeed it has scaled down with the successive advances in the physical dimensions of the basic hard disk components. However, very slim pulses are virtually impossible to detect, since they inherently imply the acquisition of negligible induced voltages on the read head at tremendous speeds. Although technological improvements in the read head and in electronic blocks regularly allow the usage of ever-thinner pulses, the obvious long term solution to this issue is to increase the amount of allowed intersymbolic interference between consecutive pulses. This naturally leads to the decrease of noise margins and eye diagram apertures. To compensate for this drawback, the dynamic range must be increased and the circuitry and coding complexity must be enhanced. Various schemes alternative to the classic peak-detect read-channels have flourished that tolerate intersymbolic interference and equalize the resulting waveshape and spectrum to a predefined target. The symbol density, also referred to as (user) bit density, packing density, or even linear density, can be directly derived from the pulse width definition used in (2.28) and can be expressed as

$$Bit_{Density} = \frac{pw50}{T} \tag{2.27}$$

where T denotes the bit interval regardless of the actual disk space occupied, i.e. the time between two adjacent pulses.

[24] See Fig. 2.15 in page 41.

The practical consequence is that the amount of intersymbol interference allowed between consecutive pulses inherently determines the amount of bits stored in a given area of the disk surface.

Lorentzian model

The Lorentzian model is the most widely used step response model of the playback process. The commonly used equation shown in (2.28) is a good approximation for most magnetic recording systems to a positive transition in magnetic polarity.

$$s(t) = \frac{1}{1 + \left(\frac{2 \cdot t}{pw50} \right)^2} \tag{2.28}$$

The corresponding waveshape is depicted in Fig. 2.11. The model is normalized to unitary peak value, and constant *pw50* denotes the pulse width at 50% of its peak value. In this example the pulse width is normalized to *pw50=2T* for a user bit density equal to 2.

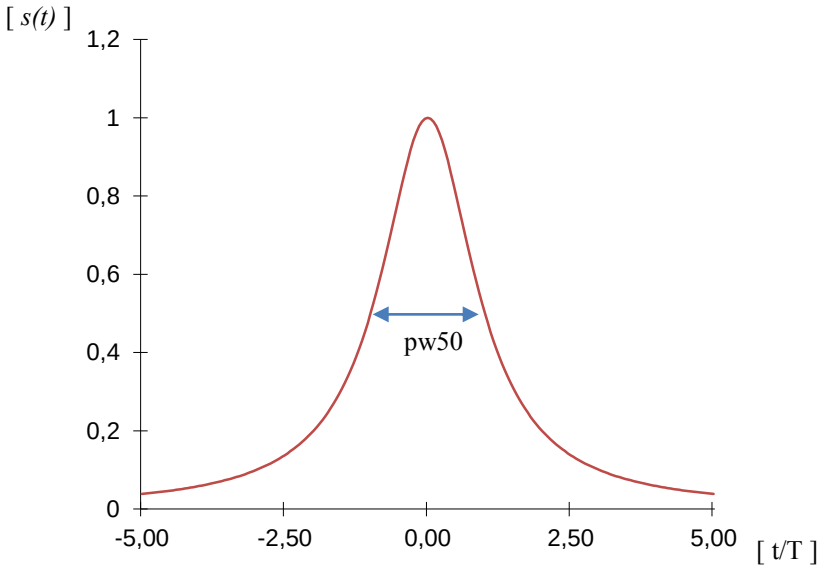

Fig. 2.11 – Lorentzian model pulse shape.

In this model, *t=0* corresponds to the instant that the read head hoverflies the boundary region of two adjacent magnets of opposite polarities. It also coincides with the read voltage peak value, and hence, for maximum efficiency given that it maximizes signal to noise ratio, most read channel architectures (e.g. peak-detect read channels[25]) use clock recovery schemes to precisely sample and decide at this instant. The portion of the response obtained for negative instants reflects the physical fact that the influence of flux transition is sensed by the read head before it actually reaches the transition boundary, thus, since this effect precedes the optimum sampling instant, it effectively corresponds to a prior awareness of a future event, and therefore is inherently non-causal. This portion of the response is usually referred to as pre-cursor response. Likewise, the post-cursor response designates the part of the waveshape that follows the transition instant.

Using the duality and time scaling principles we can derive that the corresponding inverse Fourier transform[26] of (2.28) is given by

$$s(t) = \frac{1}{1+\left(\frac{2\cdot t}{pw50}\right)^2} \quad \rightleftharpoons \quad S(f) = \frac{\pi \cdot pw50}{2} \cdot \ell^{-|\pi \cdot pw50 \cdot f|} \tag{2.29}$$

The amplitude representation of *S(f)* illustrated in Fig. 2.12 depicts the frequency behavior of the physical medium, naturally it is inherently akin to a low-pass behavior. The frequency axis is normalized to fs=1/T.

[25] See page 58 for a detailed description of the peak detect read channel architecture.

[26] Consult Oppenheim [2.4]

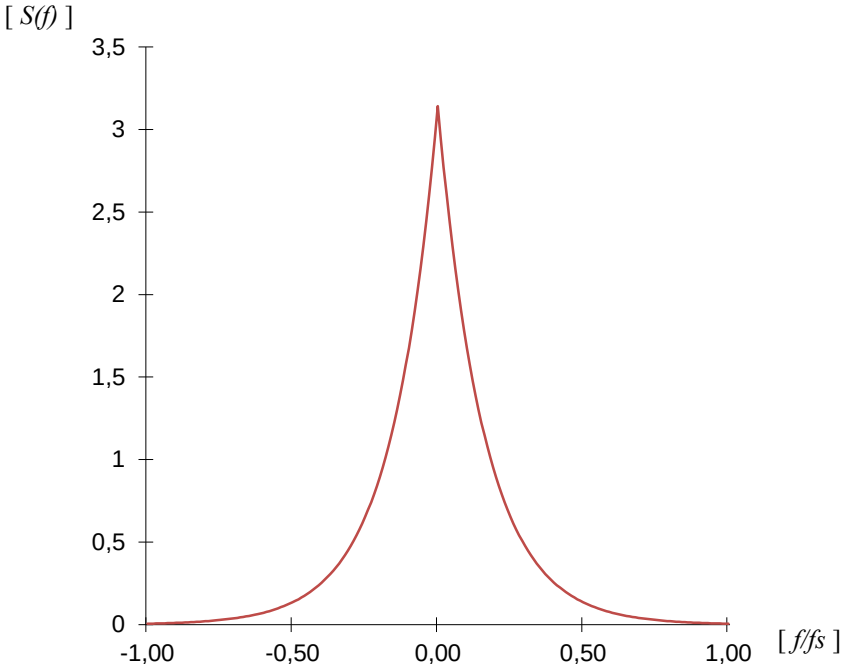

Fig. 2.12 – Lorentzian model amplitude spectrum.

Alternative models

Other alternative models for the read head response like the Gaussian model

$$g(t) = \ell^{-\pi \cdot t^2} \quad \rightleftharpoons \quad G(f) = \ell^{-\pi \cdot f^2} \tag{2.30}$$

or the Sinc model

$$s(t) = sinc(t) \quad \rightleftharpoons \quad S(f) = rect(f) \tag{2.31}$$

are compared in Fig. 2.13.

[s(t)]

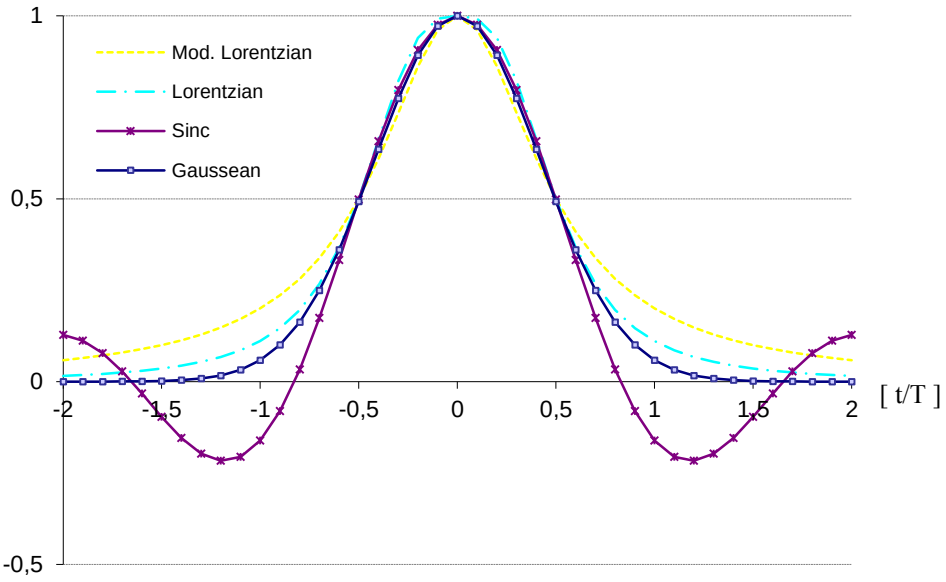

Fig. 2.13 – Normalized read head step response models.

Dibit response

The pulse response, often called dibit response of the channel corresponds to a *doublet pulse* input on the media. The magnetic head used during the write procedure carries out the playback process on a consecutive transition positive and negative transition as can be expressed by (2.33)

$$p(t) = s(t) - s(T - t) \tag{2.32}$$

doublet pulse can thus be represented as

$$p(t) = \frac{1}{1 + \left(\frac{2 \cdot t}{pw50}\right)^2} - \frac{1}{1 + \left(\frac{2 \cdot (T - t)}{pw50}\right)^2} \tag{2.33}$$

The pulse response of the read back process depicted in Fig. 2.14, effectively corresponds to the sensed voltage of two consecutive opposite polarity magnetic impulses.

[*p(t)*]

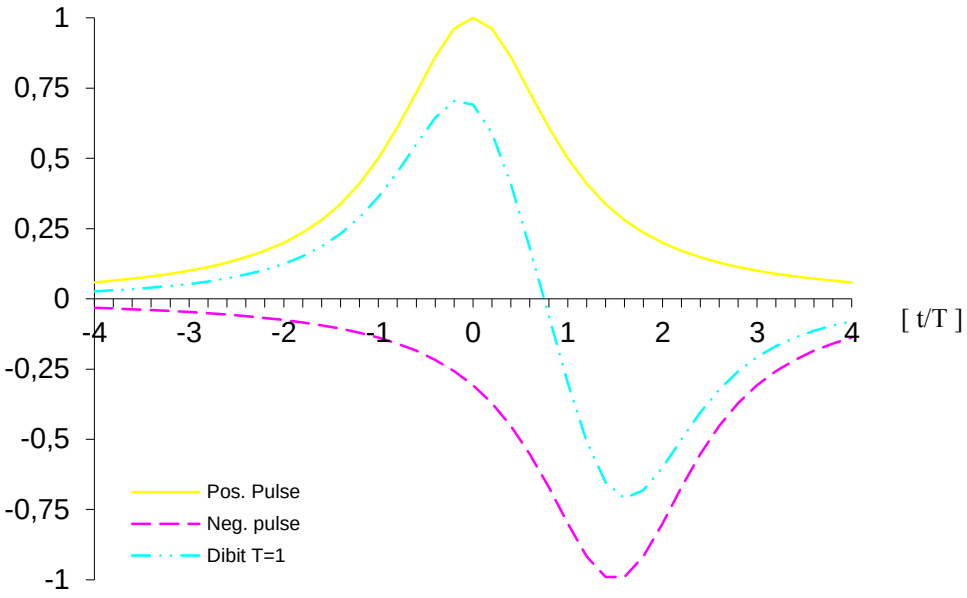

Fig. 2.14 – Dibit pulse shape.

A simple scaling of the time variable shows that the waveform obtained in Fig. 2.14 is independent of the bit interval and of the pulse width, dependent on the bit density. The waveshape is normalized to the Lorentzian pulse width at half height. The use of more aggressive bit densities lead to different dibit responses, as are depicted in Fig. 2.15.

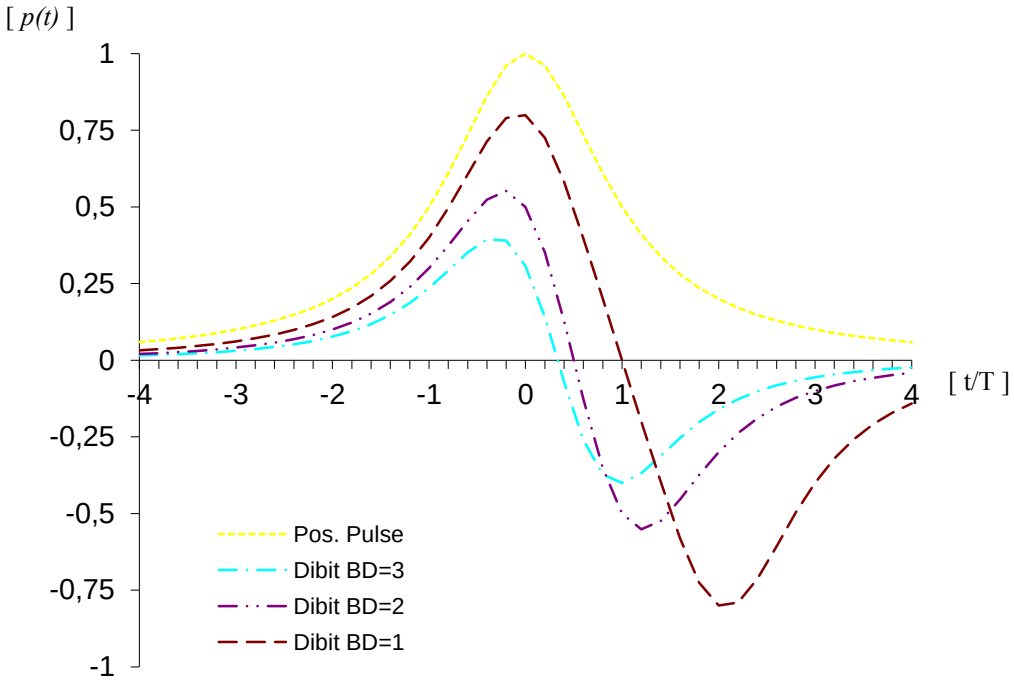

Fig. 2.15 – Dibit pulse shape for different bit densities.

As previously stated, this figure shows that the use of high bit densities severely reduces the peak values of the sensed voltage. Also noticeable is a significant phase shift of the impulses in respect to the ideal sampling instants.

Table 2.1 – ISI influence on peak value shift and decrease.

Bit density	*Peak*	*Peak shift*
1.0	0.80	- 0.1 T
2.0	0.55	- 0.2 T
3.0	0.40	- 0.3 T

Offtrack interference

The accurate positioning of the read head exactly centered on track[27] is a crucial and continuous task, both during the write and read processes. A nearly permanent monitoring and control of the servo actuator position, usually achieved through specific circuitry and predefined disk zones, secures this and other important tasks. Abbott *et al*. [2.9] performed a meticulous comparative analyzes of this effect on the most relevant magnetic recording and playback architectures.

2.7 Disk-drive electronics

The read/write process is long and complex (strongly contrasting with the apparent user simplicity to access and store information) starting out on the media magnets all the way to the CPU and vice versa. Several electronic blocks are necessary to assure proper bit detection. Fig. 2.16 represents the functional and electrical block diagrams common to most disk drive system architectures.

[27] Consult references [4.30] and [6.9] for further insight on this servo IC.

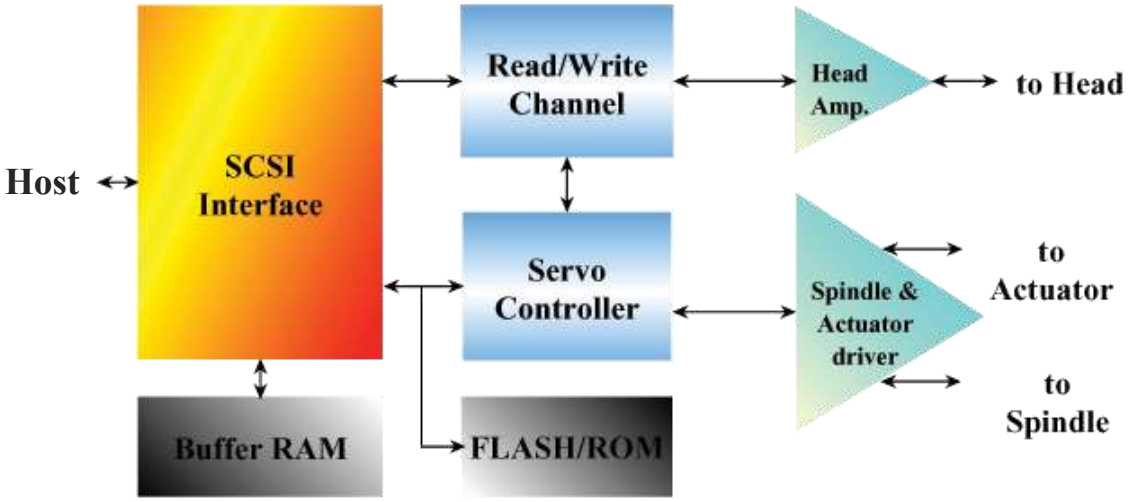

Fig. 2.16 – Disk-drive electronic blocks diagram.

The basic building blocks are the host interface DSP, the read/write channel and the servo controller. These blocks are usually assisted or include auxiliary elements for non-volatile and short-term memory and front-end drivers for the head, and for the actuator and spindle motors. Consistent endeavor for cheaper solutions in the last decade reduced the number of required integrated circuits from a dozen components including ASICs to just three or four ICs, corresponding to the basic functional blocks.

Head pre-amplifier

- **Head pre-amplifier** drives the head (with a current up to 100mA) during write and amplifies the input pulse during read. The read pre-amplifier[28] is a 40dB gain wide-band device, yielding Signal-to-Noise Ratios (SNR) of 22 to 25 dB. This component is responsible for 4% of total disk consumption and it is usually implemented in BiC-MOS or bipolar technology.

28 With very low input noise levels such as $0.5\eta V/\sqrt{Hz}$, thus the head pre-amplifier is usually mounted on a single chip very close to the read head.

Read/write channel

- **Read/write channel** is composed of two separate channels: the **read channel**[29] extracts the clock, equalizes[30] de input read head pulse, makes the digital decision and encodes data; the **write channel** basically decodes data. This block is responsible for 8% of total disk power.

Host interface

- **Host interface** usually SCSI, controls data interface between the read/write channel and the CPU, handling interrupts, and data transfer protocols. Auxiliary **Buffer RAM** chip is used for *caching* and queuing data, providing long data-bursts to improve speed and reduce bus latency. This complex digital CMOS chip takes 18% of total disk power needs.
- The remaining components take about 5% of power (e.g. ROM/PROM[31] regulators, oscillators, discrete resistors and capacitors).

Servo controller

- **Servo DSP** calculates actuator trajectories for the positioning and maintaining of the read head on track. This digital CMOS chip uses 13% of disk power.
- **Spindle and actuator driver** is responsible for driving the head actuator and the spindle motor, it is usually implemented with power CMOS, and consumption is about 10% of total power needs.

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[29] See Chapter 3 for a description of the different implementations for the read channel.

[30] This work will focus on this block, particularly in one of the key components, the pulse-slimming equalizer.

[31] Assists the *Servo DSP* and *Host Interface* chips

2.8 Market trends and evolution

Although hundreds of companies have manufactured hard disk drives, recent consolidations have concentrated production into just three main manufacturers: Western Digital, Seagate, and Toshiba. The estimated 2012 market shares are about 40% each for Seagate and Western Digital and 15-20% for Toshiba.

Worldwide revenues for HDDs shipments have reached $38 billion in 2012, for 673 million units (prices and production are back to normal since the production drop and price doubling due to the impact of Thailand flooding on HDD production capacity in 2011).

The constant quest for higher capacity (with less disks), lower power, lower supply voltage, faster devices, has pushed linear density and rotation speed up along with the (desirable) decrease of the disk size[32]. Clearly there are three different markets for hard disks:

High End (high performance & high power) tend to get faster data rates and huge storage capacity and are usually used on expensive workstations. These devices often use BiCMOS on critical components (such as the read channel).

Mid-Range (medium performance & power) follow high end drives not from far in capacity and data transfer speed, and are the desktop computer winners due to good performance/cost ratios.

Low End (low performance & low power, especially PCMCIA) drives tend to reduce device size, and power consumption and are the best choice for the booming market of battery-powered portable computers. This is the targeted application of the solutions studied in this work.

Table 2.2, and figures Fig. 2.17 and Fig. 2.18 show available data on technology advance on commercial high end drives between 1988 and 2002, clearly demonstrating

[32] From 3.5” to 2.5”, 1.8” or even 1.3” for *Low-End* drives

the exponential growth achieved on data-rate and disk capacity (and even on power requirements!).

Table 2.2 – High End disk evolution.

Year	Access Time	Disk Size	Data Rate	Disk Capacity	Total Power[33]
1988	30 ms	5.25”	3 MB/s	0.6 GByte	28 W
1990	18 ms	3.5”	3 MB/s	1.0 GByte	20 W
1992	10 ms	3.5”	5 MB/s	2.0 GByte	12 W
1994	6 ms	3.5”	10 MB/s	5 GByte	7 W
1996	-	3.5”	12 MB/s	9 GByte	5 W
1998	-	3.5”	-	18 GByte	-
2000	-	3.5”	-	36 GByte	-
2002	-	3.5”	-	72 GByte	-

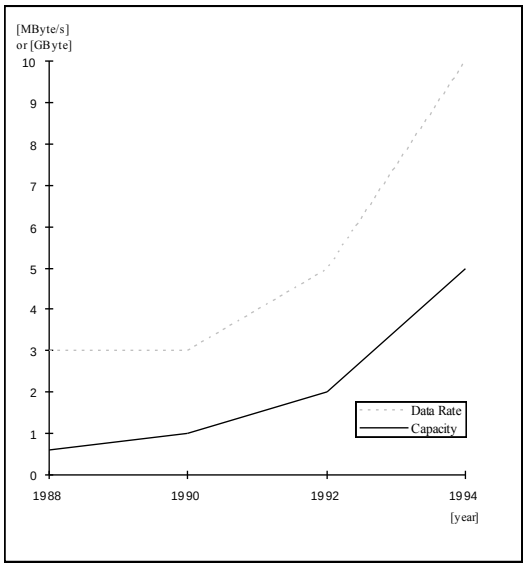

Fig. 2.17 – Storage Capacity and Data Rate evolution for *High End* drives.

[33] Power on IDLE

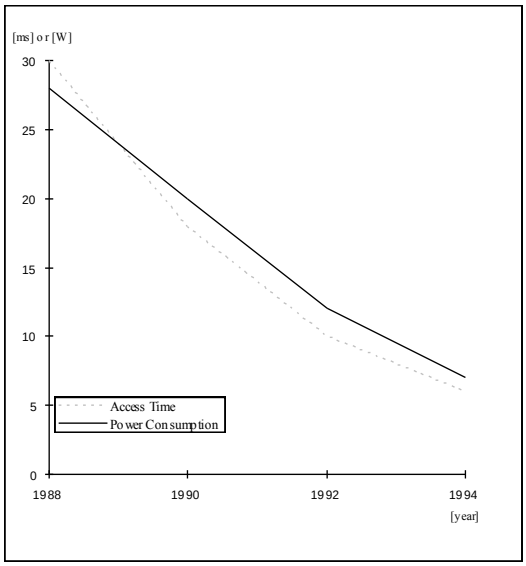

Fig. 2.18 – Consumption and Access Time evolution of *High End* drives.

Table 2.3, and figures Fig. 2.19 and Fig. 2.20 show a comparison on device size, power and volume of high end versus low end drives. The values for storage capacity and data rate for low end drives are still quite modest when compared to their high end rivals.

Table 2.3 – Low End disk drive evolution.

Year	Disk Size	Total Device Volume	Total Power
1988	3.5”	403 cm^3	8.0 W
1990	2.5”	126 cm^3	2.5 W
1992	1.8”	59 cm^3	1.0 W
1994	1.3”	20 cm^3	0.5 W

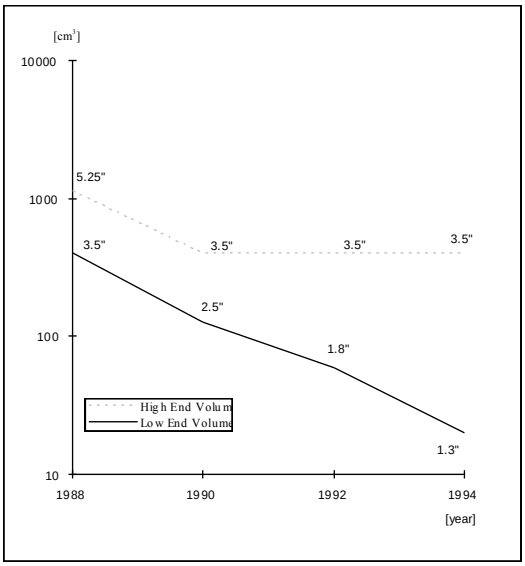

Fig. 2.19 – Size evolution.

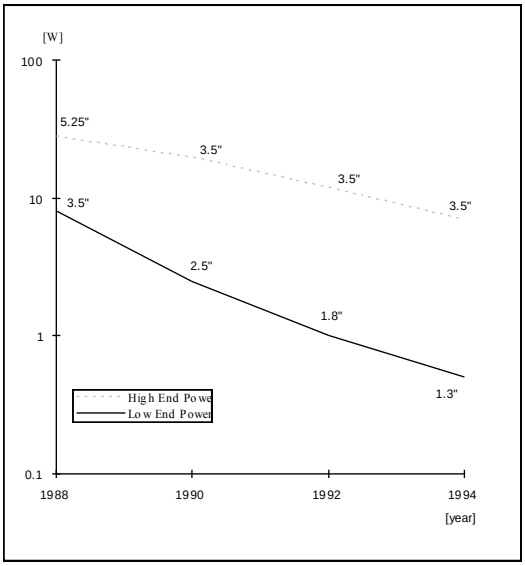

Fig. 2.20 – Consumption evolution.

2.9 Conclusions

The overall development goal in disk drive technology is clearly to reduce device size and power consumption, and to increase data rates and storage capacity. An approx-

imately exponential evolution has characterized the market offers in each of these requirements. Portable computers are the growing and profitable market off the coming years, and accordingly *Low end* drives come out as the most interesting area of study.

Low end drives aim especially at low power operation and reduced volume devices (preferentially using single disk drives), at the cost of low capacity. *High end* and *Medium performance* drives are also reducing power and size, but at lower rate focusing mainly on huge capacity devices and fast data transfer rates.

The predictable future for Low-Performance drives is that a low power single mixed signal CMOS integrated circuit will include all the referred electronic blocks (except for the spindle and head drivers) and substitute the actual 7 to 12 chip solutions with simpler and cheaper 2 or 3 chip implementations.

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Chapter 3

Coding techniques and read channel architectures

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3.1 Introduction

Although taking *only* about 20% of the total power requirements of a hard disk drive electronic interface, the read channel has been one of the most important research areas in the continuous strive for faster acquisition at lower supply voltage and most of all at extremely low consumption. The increase of data acquisition rate has forced the sampled-data schemes to enhance performance through the use of parallelism [3.1] thus high complexity and power incompatibility with low-end drives. This chapter is a study and comparison on the performance and requirements for the existing read channels in disk-drive electronics. The coding methods used in some of these read schemes will also be described.

Although digital *bits* are the essence of data storage and recovery, different techniques are employed in data coding for the achievement of optimal performance either in data rate, error probability, noise immunity and ISI forbearance. Several coding procedures and data constrains have been used (and even combined) in magnetic read channels as a result of this effort, and the read channel topology greatly depends on the chosen coding strategy. The most common coding schemes and constrains are described in this section.

With the growing need for high data storage densities on hard disk drives, conventional peak-detection acquisition front-ends gave way to more reliable data schemes. Various data recovery schemes based on DFE [3.2][3.3][3.4][3.5] and PRML detection [3.6][3.7][3.8] have been presented. These complex circuitry systems compensate the inevitable Inter Symbolic Interference (ISI) that comes with high-speed acquisition, sharpening the magnetic-head data input-pulses, mainly at the expense of high silicon area (thus high cost) and (unfortunately) high power consumption especially on high frequency channels.

3.2 Filtering and equalizing

The concepts of filtering and equalizing are closely related either in their definition as well as in their physical implementation. Filtering an electrical signal means that the frequency properties of the signal are to be affected, either through the rejection or

through the transmission of a specific signal band. The range of frequencies in which the signal magnitude is roughly unaffected is called the passband of the filter, and the range of frequencies in which the signal is strongly attenuated is called the stopband of the filter, whereas the transition band refers to the range of frequencies in the middle of these well-defined regions, where the attenuation varies in a hopefully steep way. To achieve high selectivity and large attenuation on the stopbands it is usually necessary to use high order filters which are larger, complex and expensive. Chebyshev approximations are frequently used as a way of minimizing ripple in the passband and narrowing the transition bands. The filtering of an electrical signal also affects its phase, although usually in a neglectable way.

The first electrical filters employing only discrete components: inductors, capacitors and resistor are called passive filters in view of the fact that they do not use any active components. Most of the early classical filter theory was developed for these designs, allowing the implementation of complex transfer functions. General purpose filter designs include lowpass, highpass, bandpass and bandstop functions, or the combination of these functions in a single filter design. Whilst circuit integration gathered most of the attention in the second part of the twentieth century, for various and obvious reasons[34], the filtering solutions started to include active components. Initially through the usage of semi-integrated filter designs based on operational amplifiers and passive elements, and briefly afterwards in fully integrated OPAMP-RC active filters with on-chip resistors and capacitors.

The equalization of a signal can be performed both in the signals magnitude as well as in the signals phase. The need for signal equalization usually derives from non-ideal characteristics of a signal path, either due to cables or wireless transmission; non-idealities in the acquisition transducers; or correction of inserted deviations such as distortion, magnitude and phase errors.

[34] such as cost worthiness, miniaturization, large scale integration, mass production

A gain equalizer is usually used to correct the systems amplitude to account for attenuation in the passband of the signal response thus compensating for distortion.

An equalizer can also be used to equalize the phase of the system response, another approach to phase equalization of a signal is to adjust the derivative of the phase in respect to the frequency also known as delay. Delay equalizers are realized using fixed-delay blocks, and are used to alter the group delay or envelope delay of a signal. Therefore, fixed-delay filters have linear phase response. Delay equalizers do not affect the amplitude response of the system hence they can be considered allpass filters. Phase and delay equalizers are used to reshape the signal in transmission systems that introduce undesirable effects usually due to distortion of transmission cables or transducers on the signal path.

3.3 Data coding

Data coding in binary systems has been successfully used in most of the conventional peak-detection[35] channels. This coding corresponds to the differentiation inherent to the inductive read head in the saturation recording process. It basically consists of encoding data according to the following expression (where *D* refers to the symbol delay in the D-Transform).

$$y_k = x_k - x_{k-1} \qquad \Leftrightarrow \qquad P(D) = (1 - D) \tag{3.1}$$

This corresponds to a ternary Pulse Amplitude Modulation (PAM) obtained from a random raw sequence of zeros and ones. Symbol "1" is encoded as alternate negative and positive voltage pulses *+1* or *-1*, complementary symbol "0" corresponds to the absence of a transition.

[35] See page 58 for a description of peak-detection read-channels.

3.4 NRZ and NRZI coding

Non-Return to Zero **(NRZ)** is a common binary coding in which ones are represented by the upper level voltage and zeros are represented by a lower voltage level, without an intermediate neutral state, as depicted on Fig. 3.1. This is a commonly used coding scheme e.g. in RS232 requiring only half the baseband bandwidth of Manchester coding. Polarization of the magnetic media in HDDs doesn't use rest states so it is inherently non-return to zero. The most usual raw coding in HDD systems is ***Non-Return to Zero Inverted*** **(NRZI)** usually inverted on ones has shown in Fig. 3.2, very common in most peak-detection read channels.

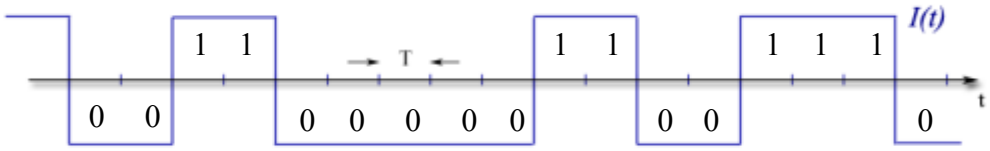

Fig. 3.1 – Non-return to zero (NRZ) coding.

Non-return to zero inverted on 1s (NRZI)

Whereas in NRZ the field direction means "one" or "zero" in NRZI a "one" means transition and "zero" means no transition. This technique is particularly useful in saturation recording. Note that if NRZI recording is used with RLL (1,k) two consecutive pulses necessarily have opposite polarities.

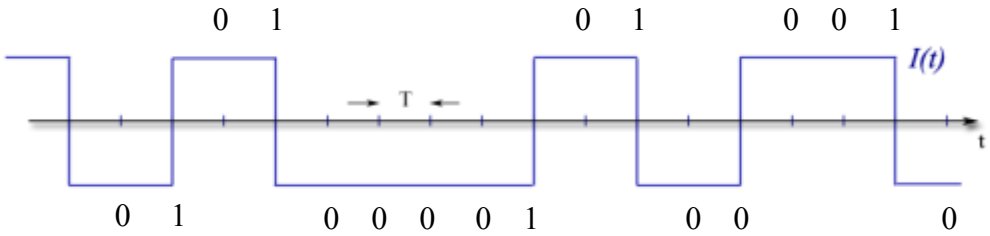

Fig. 3.2 – Non-return to zero inverted (NRZI) on ones coding.

$$NRZI = (1 \oplus D) \tag{3.2}$$

3.5 Run-length limitation

Run-Length Limitation (RLL) has been widely employed in data coding, especially in optical and magnetic recording. This coding technique is characterized by two integer constrains (*d*, *k*).

> The ***d* constrain** • *minimum run-length constrain*, imposes that transitions between different symbols occur at least *d+1* apart from each other (i.e. no less than *d* equal consecutive symbols are allowed).
>
> The ***k* constrain** • *maximum run-length constrain*, imposes that a transition between different symbols occurs at most *k* symbols after the previous one (i.e. no more than *k* consecutive equal symbols are permitted).

The *d* constrain enforces that a minimum number of zeros between consecutive ones enforcing at least *d* consecutive zeros must occur in between ones. In any case consecutive sequences of ones are not tolerable in NRZI coding due the *d* constrain.

The *k* constrain avoids long unvarying sequences of consecutive zeros, that can lead to the loss of synchronism between the clock recovery circuitry driving the detection block and the transmitted data. This is a typical problem of asynchronous data transmission systems. Since NRZI coding – the generally used coding in magnetic recording – codes zeros as *no-transition* and ones as *sign-transitions*, only a long series of zeros would inevitably lead to the loss of synchronism.

The coding rule for RLL (1,7) is given by (A B) $\rightarrow$ ($\bar{A}\,AB\,\bar{B}$) except for (A 0 0 B) $\rightarrow$ ($\bar{A}\,AB\,\bar{B}$ 0 0 0) corresponding to Table 3.1. The d constrain imposes a limit on the number of consecutive ones, hence consecutive transitions of polarity field on the media. This is achieved by the mapping two data bits on to three bits on disk, hence at the cost of reducing usable disk space and transfer rate by one third. The resulting usable disk space and transfer rate for this coding is 2/3. The maximum number of consecutive zeros is seven.

Table 3.1 – RLL (1,7) coding.

A	*B*	Coding
0	0	1 0 1
0	1	1 0 0
1	0	0 0 1
1	1	0 1 0
0 0 0 0		1 0 1 0 0 0
0 0 0 1		1 0 0 0 0 0
1 0 0 0		0 0 1 0 0 0
1 0 0 1		0 1 0 0 0 0

3.6 Peak detection channel

This is the conventional technique for data acquisition, dominating the inertial read channel market since the appearance of disk drives. This non-linear read scheme combines the lowest implementation cost with high efficiency in RLL channels, especially for low-density disks. The key block of a peak detection channel (see Fig. 3.3), the peak-detector, looks for a zero crossing in the differentiated input signal to sample the input in its local minimum or maximum value (centered on what is called the *timing window*), with acceptably high accuracy and noise immunity. A peak is detected if the module of the input value is greater than a threshold voltage (usually half the maximum amplitude), thus corresponding to a recorded symbol “1”, otherwise the output of the detector will yield the symbol “0”. The equalizer block is used as a pulse-slimming filter for improved performance, usually a high-frequency boost linear filter with low noise enhancement. The clock recovery and decoder blocks synchronize and decode the user data.

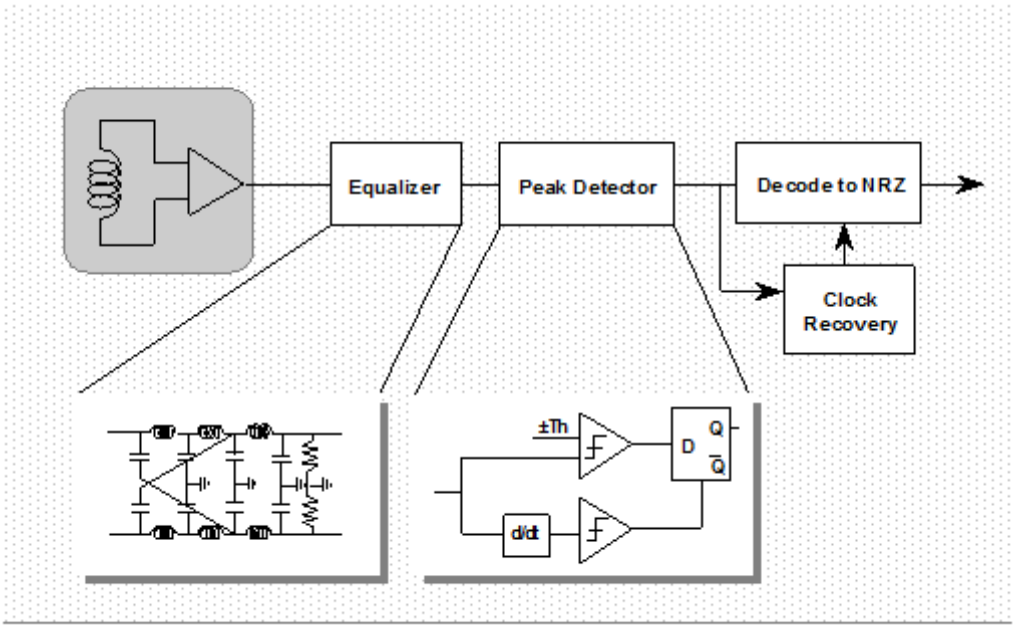

Fig. 3.3 – Peak detection block structure.

This method works for large peaks but, as data density increases, the flux reversals are packed more tightly and the signal becomes much more difficult to analyze, because the peaks get very close together, lose amplitude, and start to interfere with each other. Hence limiting the areal density on the disk so that interference does not occur.

The main features of this scheme are simplicity, low power and low area. However the push for higher speed and higher density, with its inherent problems, such as timing errors, *peak shifts*, *peak drops* and especially the increase of ISI, has made alternative read channel schemes flourish, and proved [3.9-3.17] them superior to the standard peek detection read channels. To solve this problem and allow for higher density values, a new approach to solving the data readback problem was developed, called partial response, maximum likelihood or PRML, that changes the way that the signal is read and decoded from the disk.

3.7 Partial response maximum likelihood channels

Partial Response Maximum Likelihood (PRML) coding in magnetic recording was first proposed by Kobayashi *et al.* [3.18] early in 1970, although only in [3.19] has it been

monolithically implemented. The main features of PRML are the increase in data rate and user bit density (hence in disk storage capacity) when compared with NRZ and RLL coding channels. Unfortunately this performance is achieved with additional complexity and high consumption especially at high data rates. Its simplified structure (usually like the one in Fig. 3.4) includes an ADC[36], a digital adaptive equalizer, and a Maximum Likelihood Sequence Detector (usually a Viterbi algorithm detector is used as an efficient approach to MLSD). The clock recovery circuitry provides the desired sampling rate and phase for the sample-hold block at the ADC input based on a feedback loop filter and a Voltage Controlled Oscillator (VCO). The keys to this scheme are fast analog to digital [3.20] and efficient ISI canceling on the adaptive equalizer.

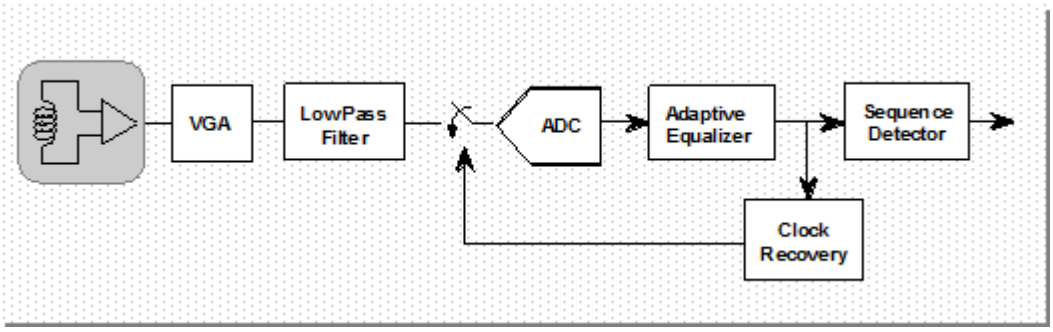

Fig. 3.4 – Block diagram of a PRML read channel.

The referred partial response (PR) coding is done in the adaptive equalizer, the key block of the channel. Different approaches to the coding are available although all of them are based on (3.3).

$$P(D) = (1-D)^m.(1+D)^n \tag{3.3}$$

Coefficients *m* and *n* determine the complexity of the equalizer transfer function each corresponding to a variant of PR (see Table 3.2).

[36] A low-pass anti-aliasing filter with near-linear phase in the passband is used prior to the sampling and conversion.

Table 3.2 – Partial response variants.

n	*m*	**Coding**		
1	0	Uncoded		NRZI
0	2	Class II	[37]Partial Response	PR-II
1	1	Class IV	Partial Response	PR-IV
2	1	Class IV	Extended Partial Response	EPR-IV

The PRML approach [3.22][3.23][3.24][3.25][3.26] differs from peak detector read channels, which do not compensate for ISI, by using advanced high-speed digital filtering to shape the read signal frequency and timing characteristics to a desired partial response, and by using maximum-likelihood sequence detection (MLSD) to determine the most likely sequence of data bits that was written to the disk.

This delay polynomial derives from the z-transform of the equalizer function where $D = z^{-1}$. The differentiating function of the read head on the NRZ pattern is usually given by (1-D) thus most PR schemes use m=1. Partial response coding based on m=1 and n=1, denominated Class IV (PR4), is a simple and elegant realization of PR, where each voltage pulse results in two samples, thus delaying the decision in time, as given by PR polynomial

$$P(D) = (1 - D) \cdot (1 + D) = 1 - D^2 \qquad (3.4)$$

Extended partial response class IV

An evolutionary improvement on the PRML design has been developed over the last few years called extended partial response, maximum likelihood (EPRML). EPRML devices work in a similar way to PRML ones, the basic principle is the same, but it uses a more complex target response polynomial also based on (3.3).

[37] For better understanding of this coding technique consult reference [3.37]

$$P(D) = (1-D)\cdot(1+D)^2 = 1+D-D^2-D^3 \tag{3.5}$$

The chief benefit of using EPRML is that due to its higher performance, linear and areal density can be increased without increasing the error rate. An increase of 20% to 70% when compared to simpler PRML designs making EPRML widely adopted in the hard disk industry and replacing PRML on new drives.

Different approaches to the coding are available although all of them are based on (3.3). An improved solution designated as extended partial response Class IV (EPR4) using m=1 and n=2 prolongs the response in time, given that each isolated pulse results in a sequence of three voltage samples (1,2,1) as a consequence of the quadratic form of term $(1+D)^2$. Further development of PR class IV designated as E^2PRML or E^2PR4 using m=1 and n=3 can increase in linear density and disk capacity, without increasing BER, but at the expense of more complex signal-processing and power consumption [3.27][3.28].

Power consumption in digital blocks is roughly proportional to the signal frequency leaving short margin for data rate increases, and hence strongly limiting their application in HDD read channels, although still showing to be robust solutions for optical data systems such as DVD/Blu-ray [3.29][3.30]. Table 3.3 summarizes the results for data rate, power consumption, and die area of relevant PRML read channel solutions.

Table 3.3 – PRML channel evolution

Year	Technology		Data Rate	Power	Area
1994	0.8μm CMOS	[3.22]	72 Mb/s	1.50 W	–
1995	0.5μm BiCMOS	[3.23]	16 MB/s	1.20 W	26 mm^2
1996	0.6μm CMOS	[3.24]	130 Mb/s	1.35 W	28 mm^2
1996	0.7μm BiCMOS	[3.25]	150 Mb/s	1.55 W	47 mm^2
1996	0.5μm BiCMOS	[3.26]	200 Mb/s	0.85 W	20 mm^2
1996	1.0μm CMOS	[3.27]	160 MHz	0.46 W	23 mm^2
1999	0.35μm CMOS	[3.28]	300 MHz	0.23 W	0.8 mm^2
2001	0.18μm CMOS	[3.29]	150 Mb/s	0.18 W	1 mm^2
2006	0.35μm CMOS	[3.30]	300 MHz	–	12.8 mm^2

High-speed acquisition and sharpening of the magnetic-head data input-pulses, is done mainly at the expense of high silicon area (thus high cost) and high power consumption especially on high frequency channels. These limitations have led to the study of alternative solutions with equivalent equalization target but based on decision feedback equalization (DFE) to avoid high frequency acquisition ADCs whereas securing ISI forbearance.

3.8 Decision feedback equalization channel

The Decision Feedback Equalization structure was the first presented in 1967, by M. Austin as an equalizing technique for dispersive channels, described in [3.2]. Adaption capability was further proposed and added to the system in 1970 by D. George *et al.* in [3.3], but it was only in 1996 that this scheme was firstly integrated in a commercial circuit as a practical alternative to peak detection techniques. This is also the main structure from which derived some of the schemes described ahead (such as FDTS/DF, RAM-DFE and MDFE). It basically consists of two equalizing filters and a slicer. The forward equalizer is typically a linear FIR filter used for *precursor* ISI cancellation and

the backward equalizer is a non-linear *post cursor* ISI remover. The non-linearity in the feedback caused by the decision element ideally enhances noise robustness, although once an error occurs it will propagate to subsequent symbols.

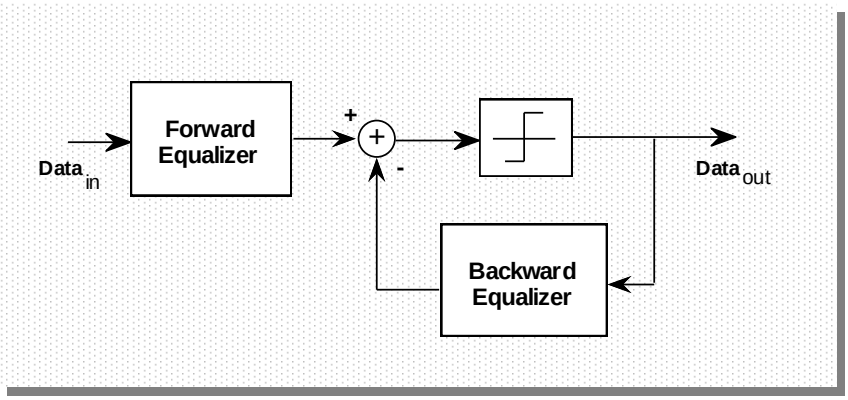

Fig. 3.5 – Decision feedback equalization block diagram.

The main feature of this equalizer is the possibility to tune both filter sections (usually using LMS modified algorithms[38]). Consequently tapped delay transversal FIR filters are the natural choice for this blocks due to their ease of implementation and tuning or programming abilities.

3.9 RAM decision feedback equalization channel

RAM-based equalization [3.5] is also used for ISI removal on storage channels, although it was first presented as a non-linear echo canceller for data modems [3.31]. This technique is particularly effective on channels for which the linear superposition is an inaccurate model. The non-linear effects on *post cursor* ISI can be canceled by detecting the sequence of the previous symbols and subtracting the corresponding RAM-stored value (for that particular sequence) from the signal at the input of the slicer. The detected sequence is temporarily stored in a shift-register whose outputs decode the RAM element that holds the expected error values. The stored values can/must be tuned recursively to

[38] see Chapter 3 for a detailed description and comparison of available tuning strategies

improve equalizing performance although this can prove to have convergence problems and comparatively higher complexity than adaptive linear equalizers. The forward filter is a linear equalizer, usually a FIR filter as those used in conventional DFE read channels.

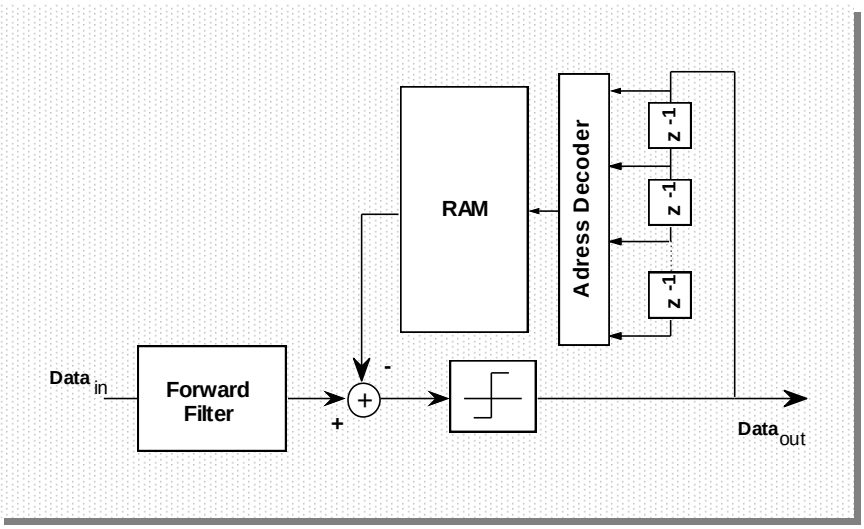

Fig. 3.6 – Block diagram of a RAM-based decision feedback read channel.

In linear echo cancellation, the assumption for canceling causal ISI using linear equalizers is that a linear superposition of the previously detected symbols will model the total echo on the current symbol. This principle suggests the use of transversal FIR filters for this purpose as was described previously. Alternatively non-linear cancellation as proposed by Agazzi *et al*. [3.31] assumes echo signals to be a non-linear function of the current and past symbols, requiring the channel to be time invariant, and also suggesting the use of memory elements. The first DFE equalizer using RAM-Based equalization was published in 1989 by Fisher *et al.* [3.4] but its hardware complexity has kept it away from the disk-drive market, moreover with the high linearity behavior of magneto resistive read heads at high densities. In 1996 Philips Semiconductors announced its first RAM-DFE read channel device based on Sands et al. [3.17] using a linear adaptive taped delay forward filter and a non-linear adaptive backward equalizer comprising a RAM element and a linear adaptive equalizer.

This work presents a 200MHz RAM-DFE channel using a linear adaptive tapped delay FIR forward filter and a non-linear adaptive backward RAM-based equalizer. Non-

linear effects on postcursor ISI can be canceled by detecting the sequence of the previous symbols, and subtracting the corresponding RAM-stored value (for a particular sequence) from the signal at the input of the slicer. Brown et al. [3.32] also proposed a complete RAM-DFE chip with 11.2mm^2 operating at 80Mb/s and dissipating 630mW using a first order continuous-time forward equalizer and a 4-tap FIR backward equalizer.

3.10 Fixed-delay tree search with decision feedback channel

The Fixed-Delay Tree Search with Decision Feedback (FDTS/DF) equalizer was first presented in 1990, by J. Moon and L. Carley [3.33] as a quasi-optimum implementation of a Maximum-Likelihood Sequence Detector (MLSD) for Run-Length-Limited (RLL) systems. The equalizer basically consists on a forward and a backward filter, along with a FTDS decision block as depicted in Fig. 3.7. Causal ISI is eliminated using a feedback filter as in DFE, but the weights of the feedback taps are smaller than its DFE counterparts thus reducing error propagation.

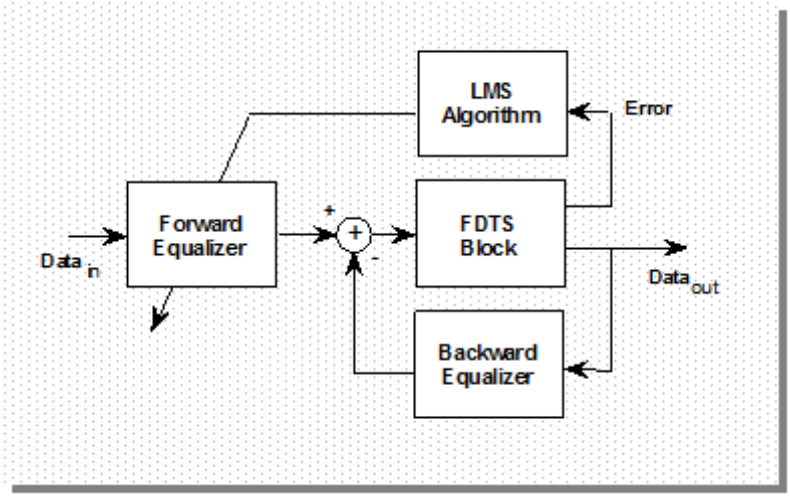

Fig. 3.7 – Block diagram of a fixed delay tree search with decision feedback read channel.

The decision delay principal is to look ahead some symbols before making the decision (according to an exhaustive tree-search, as shown in Fig. 3.8), and find the most likely path (the one that minimizes the Euclidean distance between predictable and detected sequences), much like a Viterbi detector. The FTDS algorithm achieves near-optimum performance in the case of RLL constrained input sequences since the critical error events are short and invalid paths are of easy detection, making it of reasonable hardware complexity and cost, with a performance close to that of MLSD.

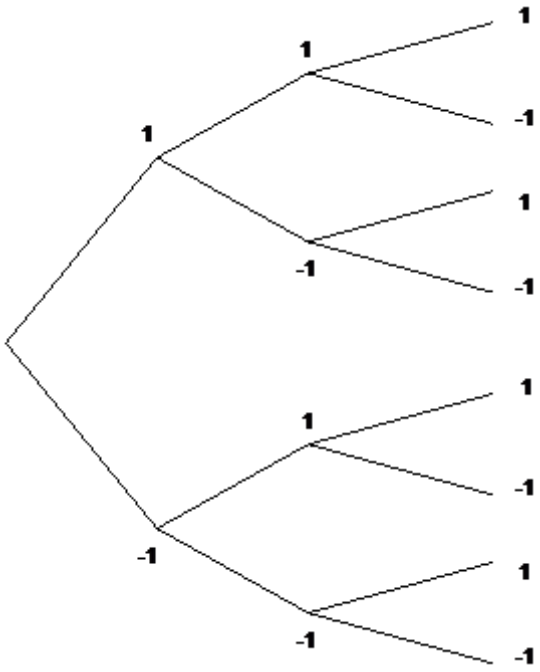

Fig. 3.8 – Binary tree search structure.

3.11 Multilevel decision feedback equalization channel

Multilevel decision feedback equalization was first proposed in 1993 by Kenney et al. [3.35] for saturation recording as a quasi-optimum implementation of a maximum-likelihood sequence detector for run-length-limited (1,7) encoded data. One interesting feature of DFE used in MDFE is the possibility to tune both filter sections. This is usually accomplished using LMS modified algorithms and can improve BER achieving S/N ratio equivalent to PR4 at user bit density exceeding 2.0. Its system block diagram is depicted in Fig. 3.9.

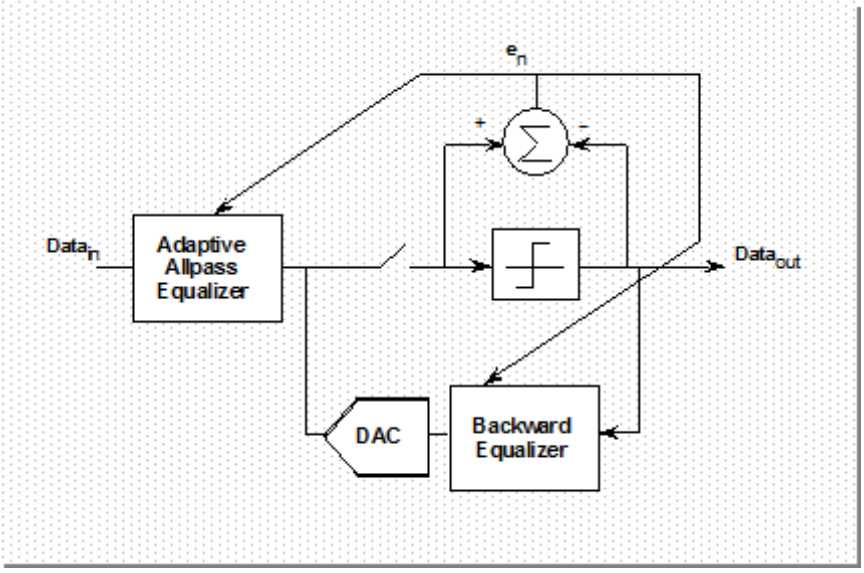

Fig. 3.9 – Block diagram of a multilevel decision feedback equalization read channel.

The equalizer basically consists on a forward and a backward filter, along with a decision element. Usually a FIR filter is used as a forward equalizer to cancel the *precursor* ISI, but recently an adaptive analog implementation [3.34] has shown its performance equivalent to that of a long (24 taps) FIR filter at lower power consumption. Causal ISI is eliminated using a feedback filter as in DFE, but the weights of the feedback taps are smaller than its DFE counterparts thus reducing error propagation.

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Chapter 4

Implementation of transconductor cells

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Pseudo-Differential Transconductor 82

Self-Biased Balanced Pseudo-Differential Transconductor 82

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4.1 Introduction

Various transconductor elements have been proposed in available literature for use in *gm*-C filters although only a few prove themselves worthy for high-frequency operation. In this chapter the basic circuits (and other more complex realizations) are compared. Expressions are derived for calculating the values of de output current and voltage, and for the value of the *gm* of the transconductance cell.

In this chapter a CMOS transconductance cell for the implementation of very high frequency current-mode *gm*-C filters is proposed and described. It features simple pseudo-differential circuitry employing small device size transistors and yielding a power dissipation of less than 1 mW/pole at nominal 3.0V supply voltage. The transconductor uses a self-biased common-mode voltage designed to minimize mismatch errors, and hence improving dynamic range and stability behavior. Short channel effects are analyzed and simulation results are presented.

4.2 Available transconductors

The basic studies for both bipolar and CMOS differential pair with passive (resistor) loads are shown in annex A. Alternative implementations usually use current mirrors to load the differential pairs leading to similar behavior but with reduced device size. A simple current mirror may not yield sufficient output resistor value hence, folded cascade structures are often employed to increase output impedance without reducing the frequency response of the transconductor cell. In these cases the circuit is sometimes called operational transconductance amplifier OTA.

Another common technique is to use cross coupled differential pairs to reduce third harmonic and total harmonic distortion of the transconductor. These are a second set of input transistors similar to the input pair but connected in the opposite direction on the drains. This technique can decrease harmonic distortion without reducing the dynamic range and frequency response of the transconductor cell as shown in [4.1], but this is not valid for very high frequency as shown in [4.2][4.3].

The implementation of the transconductance for the desired high-frequency operation led to a study of available circuits and finally to the development of a transconductor based on a pseudo-differential structured *gm*.

4.3 Differential pair transconductor with active load

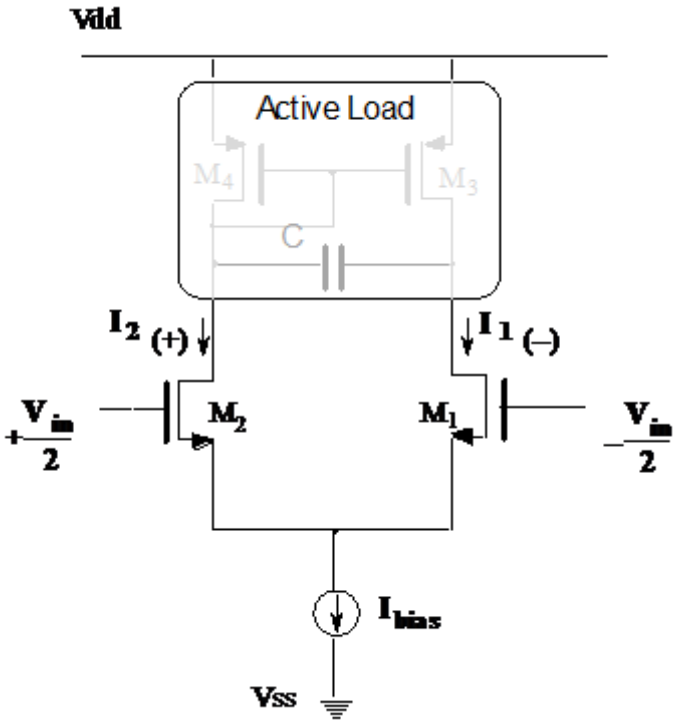

Fig. 4.1 – Schematic of a source-coupled differential pair transconductor.

The source-coupled differential pair transconductor depicted in Fig. 4.1 is the basis from where all other more complex CMOS structures have evolved. The source-coupled pair derived from its bipolar counterpart, the emitter-coupled differential pair (also the foundation for most of the common operational-amplifiers). It is a very simple and well

known device consisting of a biasing current source (I_{bias}) and two source-coupled transistors. The output currents (I_1 and I_2) usually drive an active load[39] (or passive if consisting only of a couple of simple resistors). The *large-signal* analysis of the source-coupled pair shows improved input voltage range (when compared to its bipolar equivalent), however insufficient for most applications.

Assuming the input transistors work in the saturation region, and simply stating that the biasing current (I_{bias}) equals the sum of currents (I_1 and I_2) yields the expressions derived in annex A and correspond to figures Fig. 4.2 and Fig. 4.3 for the current outputs and for the differential current output respectively.

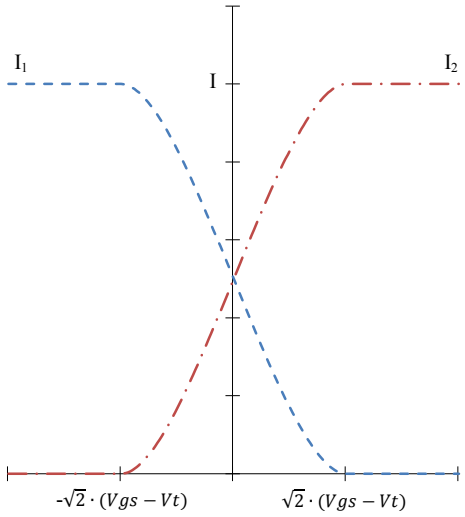

Fig. 4.2 – Current output of a differential-pair transconductor with active load.

[39] The resulting voltage output is often amplified in OPAMPs and OTAs through the use of cascode active-loads.

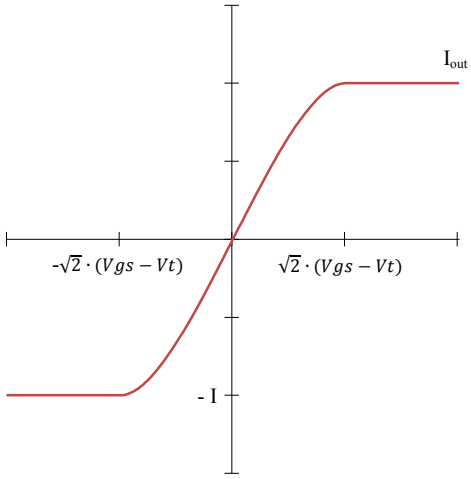

Fig. 4.3 – Differential output of a differential-pair transconductor with active load.

Figures Fig. 4.2 and Fig. 4.3 are plots of I_1 , I_2 and I_{out} for typical values of the biasing current source. It is clear that the near-linear region of operation for this transconductor is limited to just a fraction of the threshold voltage of the NMOS transistor[40], which can be improved with an high biasing current or, as will be explained, using a degeneration resistance at the source of the input transistors.

Transistors M_1 and M_2 work in the saturation region thus the output directly determine the value of the transconductance[41] (gm), in this case it will be equal to

$$gm = \mu C_{ox} \frac{W}{L} (Vgs - Vt) \qquad (4.1)$$

[40] The same can be shown for the emitter-coupled bipolar implementation, but the higher threshold values of CMOS devices give them a better range of input voltage over which the circuit can work with little distortion, thus improving the signal to noise ratio (SNR).

[41] The gm parameter of a saturated transistor is given by $gm = \frac{\partial I_d}{\partial V_{gs}}$

4.4 Differential pair with source degeneration transconductor

This source degenerated transconductor cell depicted in Fig. 4.4 is based on the source-coupled differential pair transconductor, were the current source is replaced by two current sources of equal value and a degenerating resistance as proposed in [4.4]. This resistance is implemented as a transistor working in the non-saturated region for increased linearity behavior. Working away from the saturation region the quadratic dependence on the drain-to-source voltage of the degenerating transistor becomes neglectable especially if R » 1/*gm*.

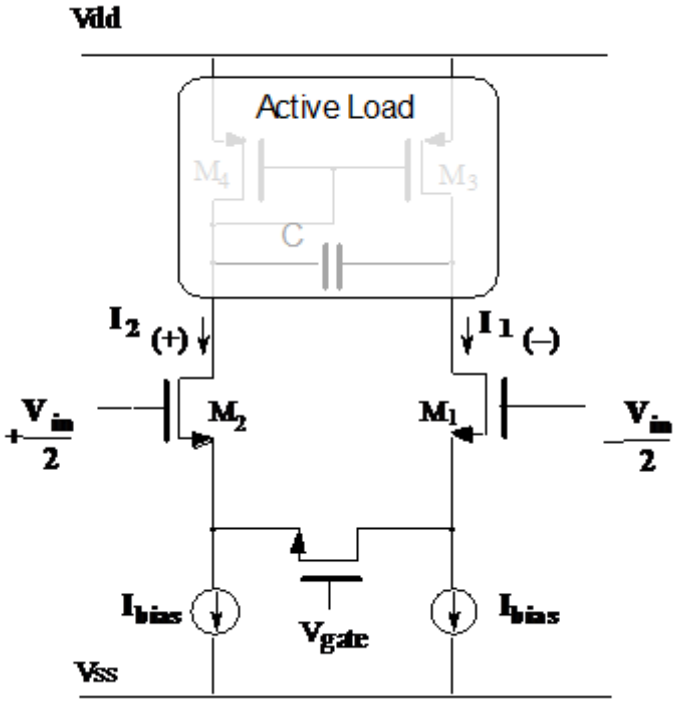

Fig. 4.4 – Schematic of a source-coupled differential pair with source degeneration transconductor.

The input transistors work in the saturation region and directly determine the value of the transconductance *gm*, in this case it will be equal to (4.2).

$$gm = \mu C_{ox} \frac{W}{L} (Vgate + Vs - Vt) \qquad (4.2)$$

Where *Vs* is the drop voltage from the input common mode voltage of transistors M_1 and M_2. A similar circuit was proposed in [4.5].

4.5 Pseudo-differential transconductor

The pseudo-differential transconductor depicted in Fig. 4.5 is an even simpler realization of the *gm* cell. The polarizing current source *I* is taken out of the circuit and the *gm* is set on the common mode voltage applied to the differential pair. This transconductor has increased voltage swing available on the output, however it usually requires additional control circuitry for the common mode voltage.

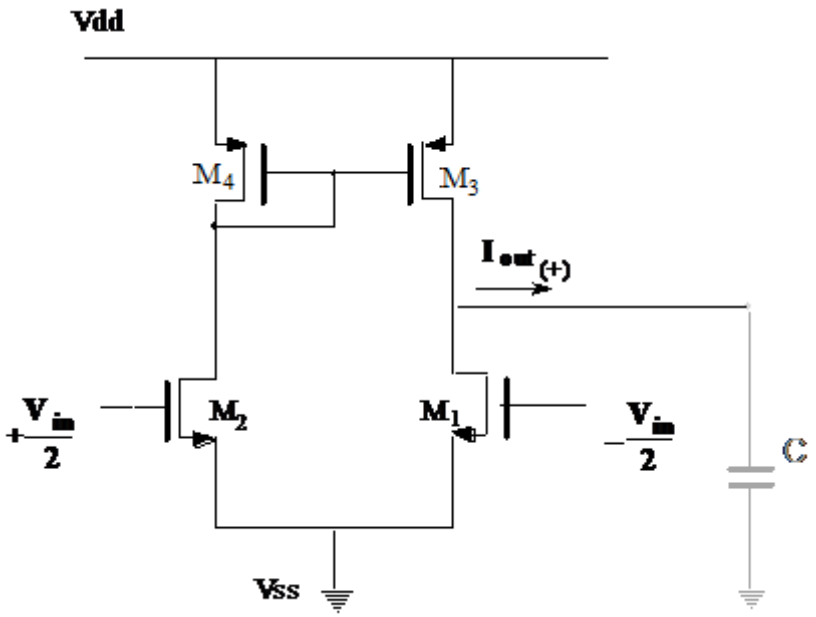

Fig. 4.5 – Schematic of pseudo-differential pair transconductor.

4.6 Self-biased balanced pseudo-differential transconductor

Most of the modern high-speed applications requiring continuous-time filtering usually employ current-mode circuit techniques to allow signal processing up to the fundamental limits of MOS devices [4.6][4.7]. Moreover, they also allow the use of plain

digital CMOS technology working at low supply voltage, which is important for the implementation of mixed analog/digital circuits. This work proposes a new transconductor cell for the implementation of very high frequency applications. It uses a pseudo-differential topology employing small device size transistors and relies on a self-biased common-mode voltage to achieve improved noise and stability behavior. This DC voltage is designed to minimize mismatch errors and is imposed by the current feedback path.

Technology assessment

In modern submicron CMOS technologies the long-channel pinch-off model usually described by the well-known square-law model is no longer valid [4.8][4.9][4.10] to accurately describe the behavior of the transistor in the saturation region. The use of short-channel devices implies that even simplified analysis should include the influence of gate (transverse) and source-drain (longitudinal) electrical fields on mobility. This is particularly relevant in deep and ultra-deep submicron technologies (e.g. 0.25μm, 0.18μm or 0.1μm) using ultrathin-oxide interfaces of SiO_2/Si, as low as 10Å. The importance of these parameters has augmented with the consistent shrink in the minimum effective channel length and gate oxide thickness of MOS transistors inherent to process advancements. The effect of the vertical electrical field is modeled by the mobility modulation parameter θ, which models mobility degradation at high gate-source voltage and depends mainly on the dioxide film thickness. The critical field for mobility degradation ξ_{crit}, which represents the limit for surface mobility, can be used to model the effect of the longitudinal electrical field. A direct effect of channel length reduction is the increase in the magnitude of the longitudinal electric field along the channel, especially near the drain. This increase results in the rise of electron energy and of scattering probability, therefore decreasing mobility. Hence, Shockley's gradual channel approximation valid for low electric-field model is not accurate enough to represent electron mobility in short-channel MOSFETs. Both parameters were introduced in Level 3 MOS modeling and are present in short-channel BSIM models for analogue and digital design. Under these conditions and including the channel length modulation parameter the transistor current can be expressed by [4.11]

$$I_d = \mu C_{ox} \frac{W}{L} \frac{(V_{gs} - V_t)^2}{2(1 + \theta \cdot (V_{gs} - V_t) + \xi_{crit} \cdot \frac{V_{ds_{sat}}}{L})} \cdot (1 + \lambda V ds) \tag{4.3}$$

Taking the partial derivative of (4.3) with respect to V_{gs} and assuming $V_{ds_{sat}} = V_{gs} - V_t$ we then obtain the following expression for the transistor transconductance

$$gm = \mu C_{ox} \frac{W}{L} \cdot \frac{(V_{gs} - V_t)}{2} \cdot \left[\frac{1}{1 + \left(\theta + \frac{\xi_{crit}}{L} \right) \cdot (V_{gs} - V_t)} + \frac{1}{\left[1 + \left(\theta + \frac{\xi_{crit}}{L} \right) \cdot (V_{gs} - V_t) \right]^2} \right] \tag{4.4}$$

From the above expression, two simpler expressions for the transistor transconductance can be derived. On the one hand, the typical simplification for long length devices biased near the week inversion region yield the well-known *gm* relationship shown in the first branch of (4.6). On the other hand, mobility reduction due to the combined effect of transverse and longitudinal electrical fields of MOS transistors is essential for short length devices biased in the strong inversion. As a result if

$$\left(\theta + \frac{\xi_{crit}}{L} \right) \cdot (V_{gs} - V_t) >> 1 \tag{4.5}$$

the expression in the second branch of (4.6) is valid

$$g_m \approx \begin{cases} \mu C_{ox} \frac{W}{L} \cdot (V_{gs} - V_t) & \Leftarrow L \geq 2.0 \mu m \wedge V_{gs} - V_t \leq 0.3V \\ \mu C_{ox} \frac{W}{L} \cdot \frac{1}{2 \cdot \left(\theta + \frac{\xi_{crit}}{L} \right)} & \Leftarrow L \leq 0.5 \mu m \wedge V_{gs} - V_t \geq 2.0V \end{cases} \tag{4.6}$$

the transistors achieve their maximum frequency behavior when approaching the velocity saturation region, where *gm* becomes nearly independent of ($v_{gs} - V_t$) overdrive inasmuch as mobility is limited by the maximum drift velocity of carriers. Near this region, the gm/I_d ratio becomes inefficient since the transconductance barely increases with the biasing current. Considering small values of L we can expect that $\frac{\xi_{crit}}{L} >> \theta$ and hence the transconductance becomes

$$g_m \rightarrow \frac{C_{ox} \cdot V_{sat} \cdot W}{2} \tag{4.7}$$

where

$$V_{sat} = \mu / \xi_{crit} \tag{4.8}$$

is the saturation velocity of carrier at nominal temperature. The gate parasitic capacitance $C_{gs}=2/3 \cdot C_{ox} \cdot W \cdot L$ and gm define a limit for the transition frequency f_t of the transistor, as given by

$$f_t \equiv \frac{g_m}{2\pi \cdot C_{gs}} \rightarrow \frac{3 \cdot V_{sat}}{8\pi \cdot L} \tag{4.9}$$

For 0.5μm devices, this value corresponds to approximately 20 GHz (NMOS) and 15 GHz (PMOS). Therefore, it is expectable that transconductors can work with negligible phase shift up to 1 GHz, and hence active transconductance-C filters operating at very high frequency can be realized.

Balanced transconductor with self-biased feedback

Several transconductor topologies have been presented that are capable of high frequency performance [4.12][4.13][4.14][4.15]. The pseudo-differential topology proposed in [4.13] is particularly interesting for the low supply voltage operation typical of modem submicron CMOS technologies, for two main reasons. Firstly, since it does not require the typical tail current of differential pairs it can provide increased headroom for the output voltage swing. Secondly, the grounded gate parasitic capacitances of the input transistors are easily absorbed in the sizing of the integrating capacitors. This circuit, however, requires additional components for the implementation of the common-mode and damping control networks. Therefore it can suffer from additional noise interference and potential common-mode voltage instability due to component mismatches. An interesting solution to overcome the problems of common-mode networks has been proposed in [4.16] and consists of achieving the required biasing by means of appropriate feedback loops without the use of common-mode circuitry. The implementation given in [4.16] requires feedback transconductance circuitry that performs the output voltage sensing, in

the first place, then a sign inversion and finally the voltage to current conversion for the input comparison. The solution proposed in this thesis is based on a pseudo-differential topology, as given in [4.13], but whose common-mode voltage is established in a simpler way than the one presented in [4.16]. As we can see in figures Fig. 4.6 and Fig. 4.7 this consists of a pure current-mode feedback path established between the output nodes (I_{d+}, I_{d-}) and the input nodes (V_{gs-}, V_{gs+}), providing exact unity common-mode feedback voltage gain. A simple first order low-pass filter example is given in Fig. 4.7, but the proposed technique is also valid for general purpose filters using more complex structures, as the ones in [4.17]. As it will be shown next, the sizing of the transistors can be obtained in order to provide an optimum common-mode voltage that minimizes the effects of component mismatches on the operation of the circuit.

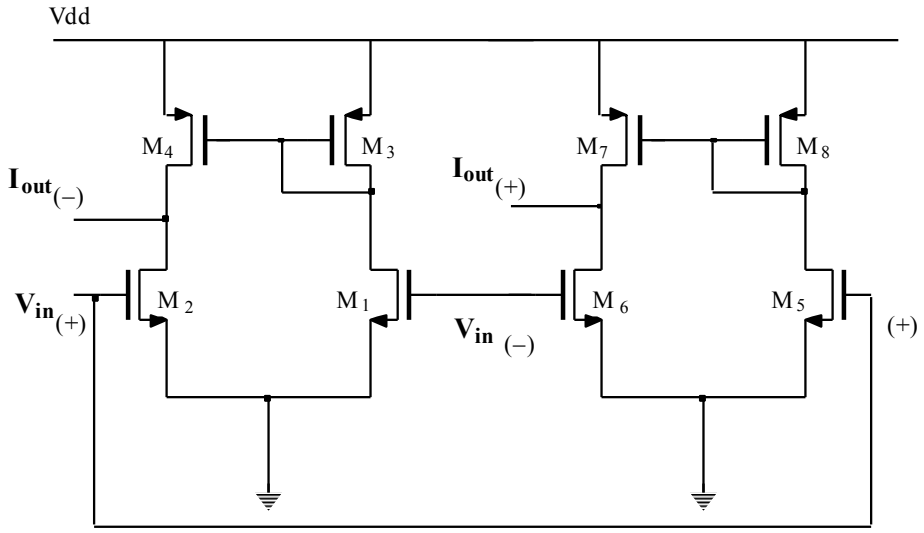

Fig. 4.6 – Schematic of *gm*.

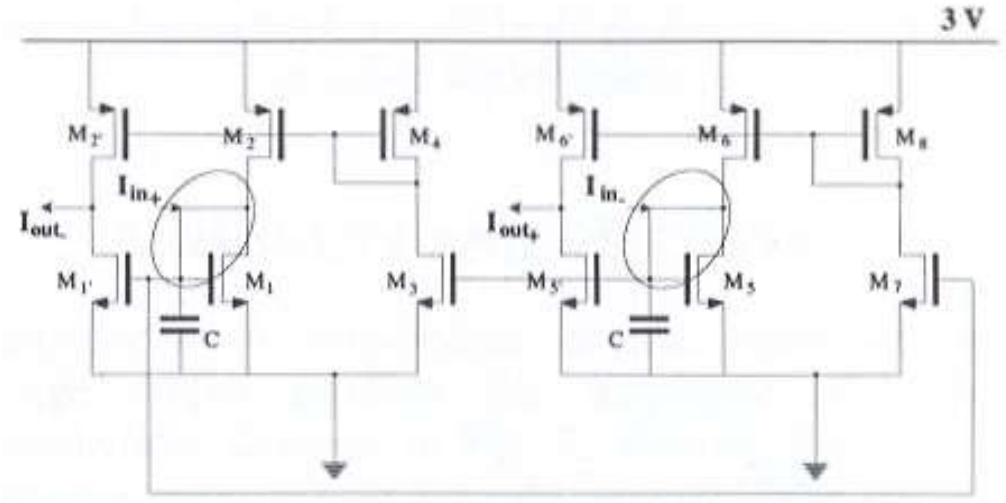

Fig. 4.7 – Self-biased connection in a first order low-pass filter.

The internal node of the active loads also stabilizes the common-mode of the transconductor, since the drains of M_1, M_2 and M_5, M_6 ideally track the DC drain voltage of M_3, M_4 and M_7, M_8 due to finite *gds* conductance. This node imposes a high frequency parasitic pole at approximately

$$f_{node} \approx \frac{g_{m_{PMOS}} \,//\, g_{ds_{PMOS}} \,//\, g_{ds_{NMOS}}}{2\pi \cdot \left(C_{gs_{PMOS}} + C_{gs_{PMOS}}\right)} \approx \frac{f_{t_{PMOS}}}{2} \quad . \tag{4.10}$$

The input voltage $v_{in} = V_{gs+} - V_{gs-}$ and the output current $i_d = I_{d+} - I_{d-}$ are fully balanced around the common-mode voltage V_{cm}, thus canceling even-order non-idealities. Hence, considering the balanced inputs $V_{gs+} = V_{cm} + v_{in}/2$ and $V_{gs-} = V_{cm} - v_{in}/2$, the output current can be derived from (4.3) and be expressed exactly by

$$i_d = \left(I_{d+} - I_{d-}\right) = \mu C_{ox} \cdot \frac{W}{L} \cdot \frac{v_{in}}{2 \cdot \left(\theta + \frac{\xi_{crit}}{L}\right)} \cdot \left[1 - \frac{1}{\left[1 + \left(\theta + \frac{\xi_{crit}}{L}\right) \cdot (V_{cm} - V_t)\right]^2 - \left(\theta + \frac{\xi_{crit}}{L}\right)^2 \cdot \frac{v_{in}^2}{4}}\right] \tag{4.11}$$

This expression can also be simplified for both long and short channel devices, yielding the expressions shown in (4.12)

$$i_d \cong \begin{cases} \mu C_{ox} \dfrac{W}{L} \cdot (V_{cm} - V_t) \cdot v_{in} & \Leftarrow \quad L > 2.0\mu m \\ \mu C_{ox} \dfrac{W}{L} \cdot \dfrac{v_{in}}{2 \cdot \left(\theta + \dfrac{\xi_{crit}}{L} \right)} & \Leftarrow \quad L < 0.5\mu m \end{cases} \tag{4.12}$$

Therefore, in both cases, the output current is quasi-linear in respect to the input differential voltage. An estimated large-signal distortion of approximately 0.2% for $v_{in}=1V$ is expected from (4.11), but real values should increase due to mismatch. Common-mode and supply rejection are only limited by the mismatch between the identical NMOS M_1, M_3, M_5, M_7 and PMOS M_2, M_4, M_6, M_8 transistors.

Optimum auto-biasing for minimum mismatch effects

Matching properties of MOS transistors show that the variance in both the threshold voltage and gain factor $\beta = \mu . C_{ox} . W/L$ affect the mismatch of I_d according to [4.18]

$$\frac{\sigma^2(I_d)}{{I_d}^2} = \frac{4\sigma^2(V_t)}{(V_{gs} - V_t)^2} + \frac{\sigma^2(\beta)}{\beta^2} \tag{4.13}$$

Since the standard deviation parameters $\sigma(V_t)$ and $\sigma(\beta)$ are approximately proportional to $1/\sqrt{W \cdot L}$ minimum size lengths lead to even stronger deterioration of matching, especially in digital technologies. Therefore, although the use of minimum length devices is advisable to achieve maximum frequency performance, a trade-off must be obtained between speed and the amount of allowed mismatch. Fabrication statistical data for both PMOS and NMOS transistors available from similar processes [4.19] suggest a minimum channel length of $0.8\ \mu m$ considering a $0.05\ \mu m$ mask pitch. This data has also been used to estimate the common-mode voltage V_{cm} that minimizes the influence of threshold voltage dispersion on the output current, yielding

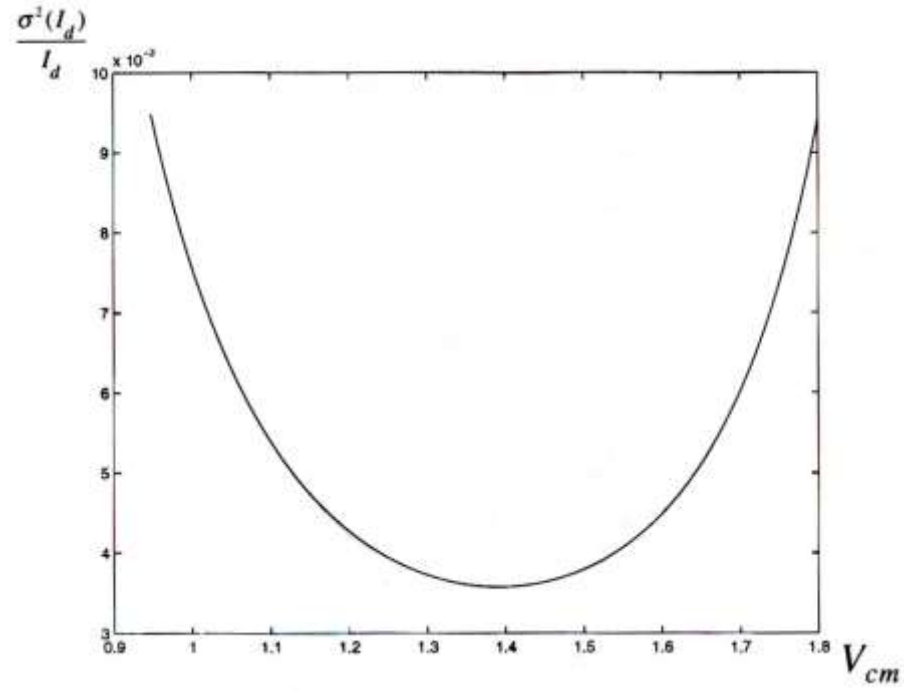

Fig. 4.8 – Ideal common-mode voltage for the *gm*.

$$\min\left[\left(\frac{\sigma^2(I_{d\,PMOS})}{I_{d\,PMOS}^{\,2}}+\frac{\sigma^2(I_{d\,NMOS})}{I_{d\,NMOS}^{\,2}}\right)(V_{cm})\right]_{VDD=3.0V} \tag{4.14}$$

hence

$$\left.\frac{\sigma^2(I_d)}{I_d^{\,2}}\right|_{V_{cm}\approx 1.4V} \tag{4.15}$$

The ideal DC common-mode voltage of $V_{cm}=1.4V$ imposes $V_{gs}-V_t = 1V$, and thus keeping the PMOS and NMOS transistors in the strong inversion region, although not far from velocity saturation. The self-biasing occurs in the intersection of the DC characteristic of the transconductor with the $V_{in+}=V_{out-}$ and $V_{in-}=V_{out+}$ constrains imposed by the current feedback paths, as illustrated in Fig. 4.9. The transistor dimensions determining the biasing voltages are calculated to locate the intersect point at $V_{cm}=1.4V$ and thus minimizing mismatch effects while maintaining maximum frequency operation.

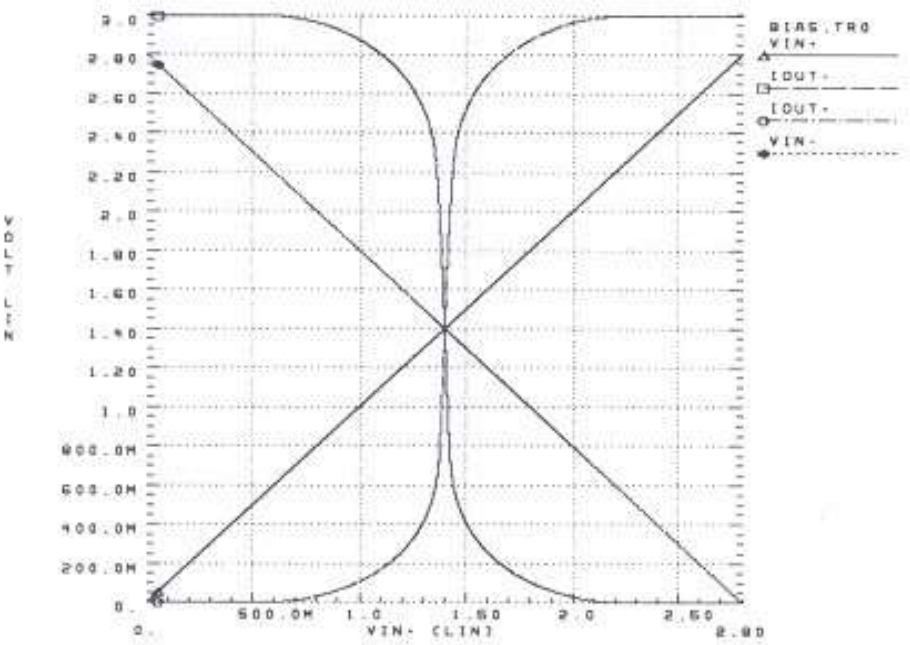

Fig. 4.9 – DC biasing is self-imposed by the feedback loops established in a filter implementation.

Noise

A brief analysis of the noise of this transconductor cell can be derived from the noise model of the MOSFET transistors. The capacitors used to implement the desired filtering functions ideally can be considered noiseless, although the non-ideal effects inherent to the implementation techniques can introduce noise.

The two types of noise usually considered for MOSFET transistors are thermal noise and flicker noise. Thermal noise is caused by the influence of temperature on the motion of electrons provoking random current flow in passive or active components. Both NMOS and PMOS transistors used in this trancondutor cell are biased in the saturation region, where this noise can be modeled as a drain noise current source with spectral density

$$S(i) = 4kT \cdot gm \tag{4.16}$$

where *gm* is the transconductance of the transistor.

Flicker noise, also known as *1/f* noise, is due to the flow of current in the device, and can be modeled as a drain noise current source with spectral density

$$S(i) = 4kT \cdot \frac{f_c}{f} \tag{4.17}$$

Distortion, PSRR and GSRR

The transconductor cell is balanced, hence the effect of pair harmonics should not be observed. The simulation prediction for the third harmonic and for THD are approximately -50dB.

To simulate the power source rejection ratio (PSRR), ground source rejection ration (PSRR), and common mode rejection ratio (CMRR) we considered deviation in the transistor models of the differential pair, otherwise ideal behavior would be obtained. To estimate CMRR we forced ±10% in Vtp and Vtn and ±10% mismatch on the input transistors to guaranty unbalance at the input differential pair. The voltage value observed at the current state variables (at the output of the transconductor cells of the filter) can be observed in Fig. 4.10. Lower than 80dB CMRR is estimated for this design. Analogous simulations where performed to calculate PSRR and GSRR estimated to be under 45dB as can be observed on Fig. 4.11 and Fig. 4.12.

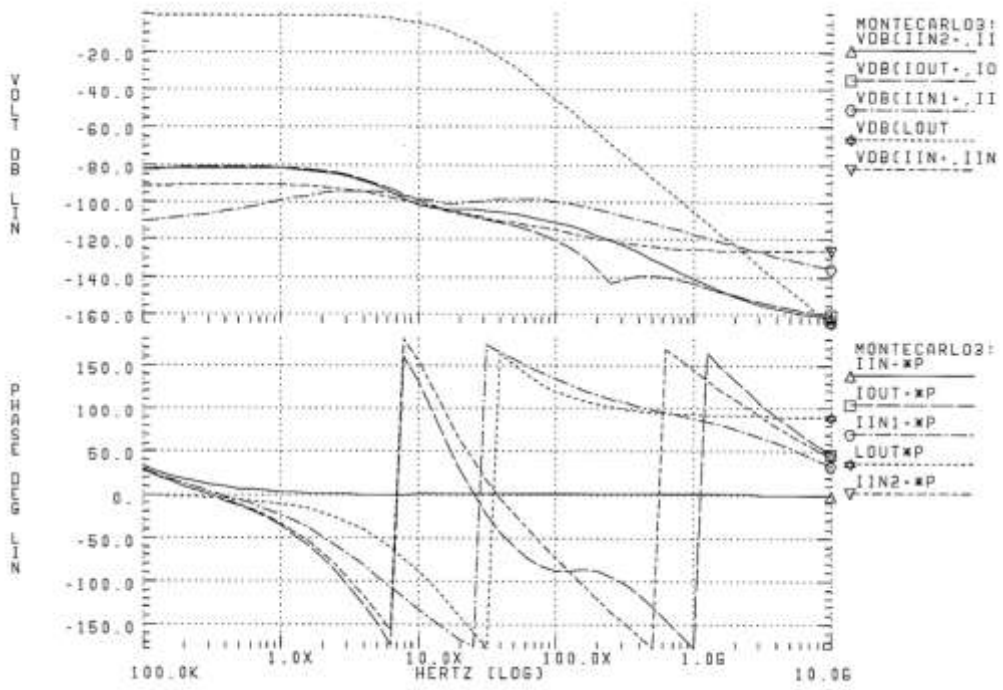

Fig. 4.10 – Common mode rejection ration of the equalizers (>80dB).

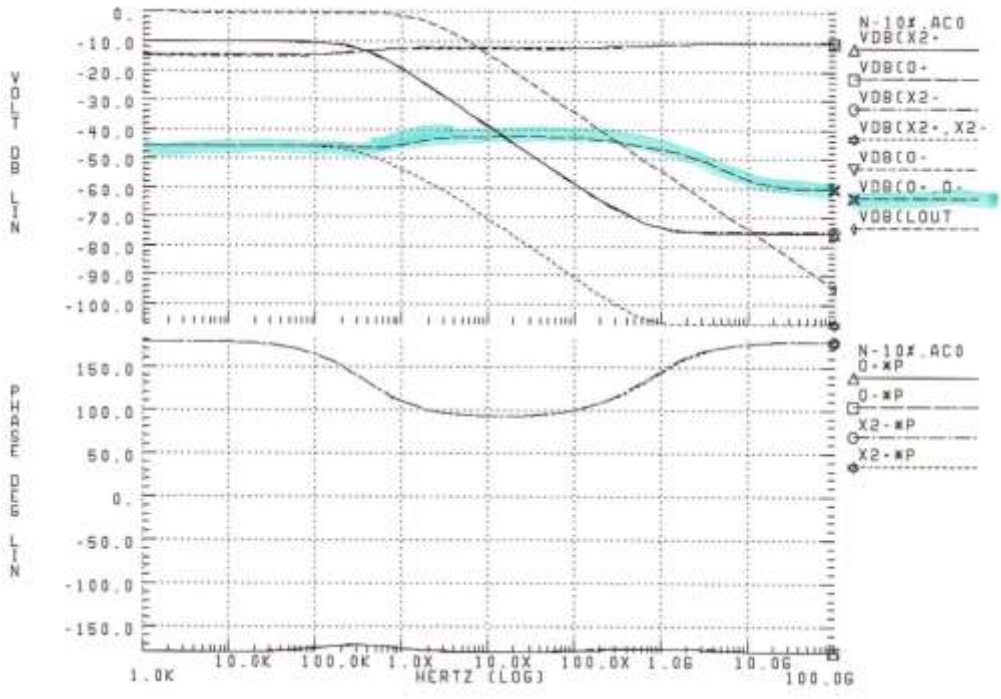

Fig. 4.11 – Power source rejection ratio of the equalizers (>45dB).

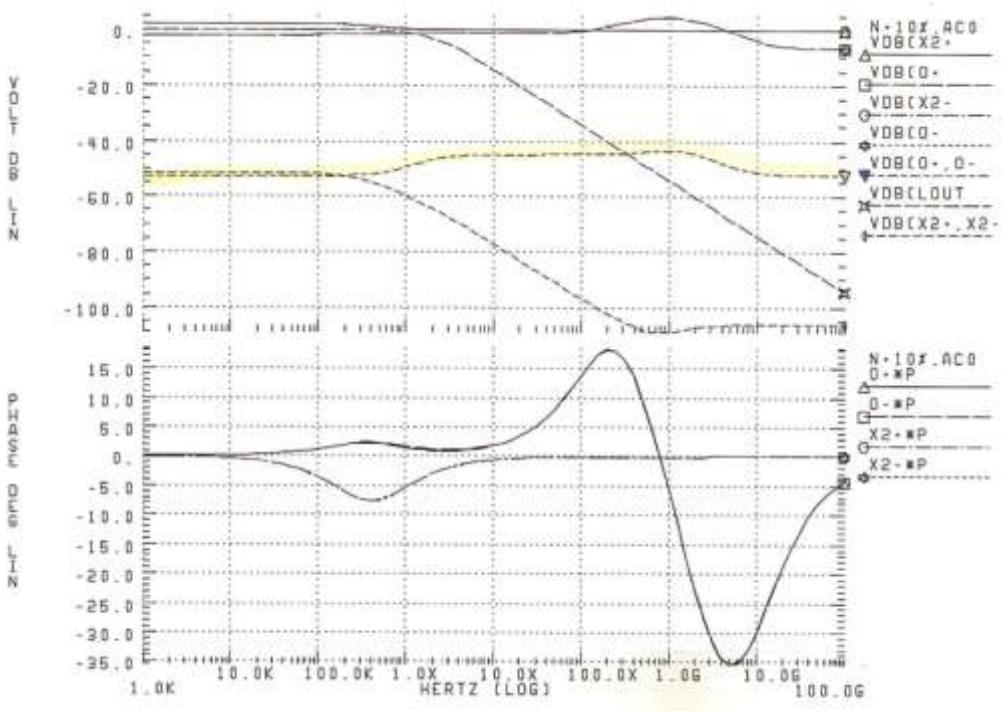

Fig. 4.12 – Ground source rejection ratio of the equalizers (>45dB).

Results and discussion

Transistor level simulations of the transconductance single-ended and differential output voltage produce the amplitude and phase characteristics depicted in figures Fig. 4.13 and Fig. 4.14, showing that the high frequency parasitic pole is located around 5GHz and close to the *ft* of the transistors. Some additional simulation results of the transconductance cell are shown in Table 4.1.

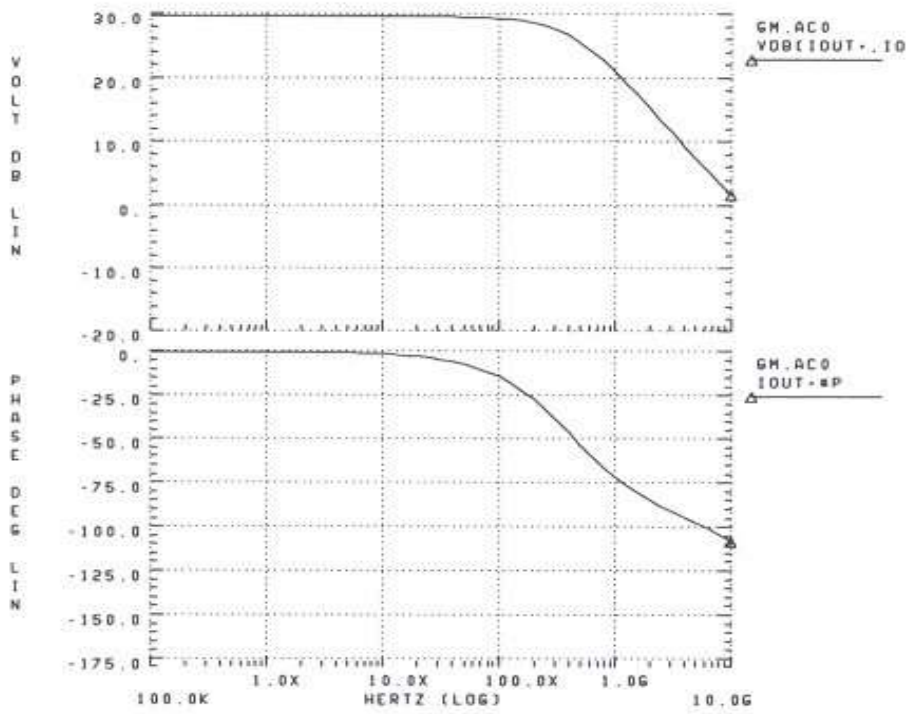

Fig. 4.13 – Frequency response of the pseudo-differential transconductor.

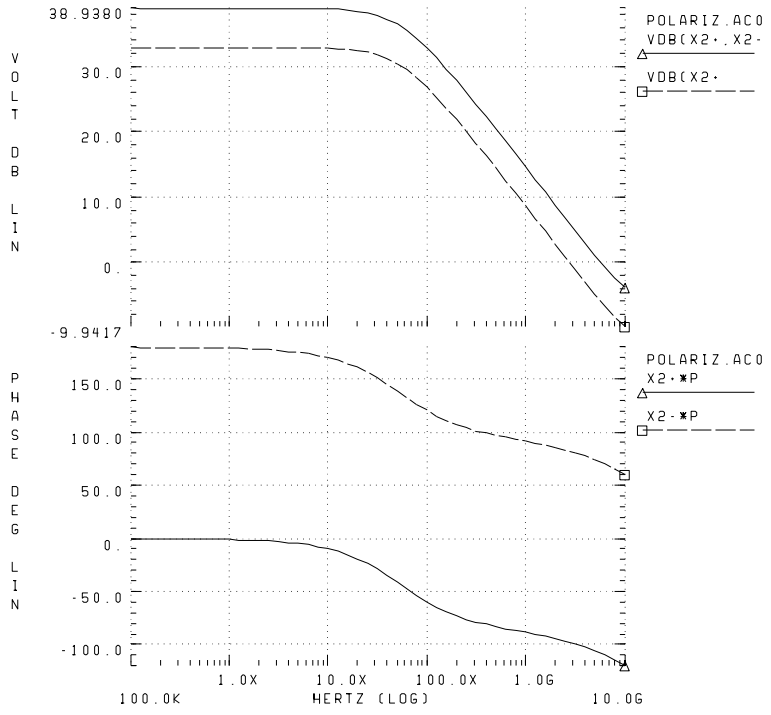

Fig. 4.14 – Frequency response of *gm* with 100KΩ output load (I_{out+} and I_{out-}).

Table 4.1 – Characteristics of the MOS transconductor.

Technology	0.5μm Digital CMOS
Supply Voltage	3.0 V
CMRR	80 dB
PSRR, GSRR	45 dB
THD ($1V_{pp}$@10MHz)	–50 dB
Power dissipation	350 μW

4.7 Conclusions

This chapter presents an auto-biased transconductor cell for the implementation of VHF continuous-time current-mode *gm*-C filters. The auto-biasing is granted by feedback loops, thus avoiding common-mode circuitry and yielding improved stability and noise immunity. The proposed transconductor can operate at low supply voltages for reduced power dissipation. The small feature transistors are designed to allow good high frequency operation while controlling mismatch effects. Computer simulations show that this transconductor is capable of sustaining correct operation for supply voltages as low as 1.8V.

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Chapter 5

Forward equalizer for MDFE read channels

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Channel architecture 106
Adaptive gm-C architectures 108
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Results and discussion 116
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5.1 Introduction

This chapter presents a comparative study of two adaptive continuous-time 3rd order allpass equalizers for magnetic disk decision feedback equalization read channels. These are based on adaptive current-mode *gm*-C structures employing low-mismatch high bandwidth pseudo-differential balanced transconductors and polarized MOSFET arrays as integrating capacitors. Transistor level simulation results are presented to demonstrate the performance characteristics of both structures. In this section different architectures for the forward equalizer will be presented and compared. The main specifications of the adaptive filter and of its critical components will be derived.

The required complexity and desirable filtering figure of an equalizer for digital acquisition varies significantly on the application both due to the physical media and peripheral components, and due to the operating frequency and coding technique employed. The need for increased data rates and higher storage capacity made quasi-raw storing insufficient and gave way for partial response coding in magnetic storage. This brought about the use of finite impulse response filters combined with fast analog-to-digital conversion. The low-resolution requirements for digital-data acquisition have allowed practical PRML solutions at relatively high frequencies, likewise simple FIR equalizers or sequence detectors with tolerable complexity and power necessities have been proposed for magnetic disk read channels.

However, the augmented constrains of more advanced partial response schemes, such as PR4 or EPR4, together with the ever-growing need for higher data-rates — which formerly drove PRML solutions from paper to market — ultimately condemn PRML to a dead on arrival condition. Although some interesting schemes where developed for high frequency specifications at reasonably low power consumption, the fundamental increase of power requirements with operating frequency akin to these architectures became an intolerable bottleneck to the system.

Decision feedback equalization architectures don't require fast analogue-to-digital conversion relying alternatively on a simple comparator decision element — commonly known as slicer — and hence, do not suffer the same fundamental power limitation of

their PRML counterparts. Nevertheless, the FIR equalizers in its architecture are also power hungry especially at high frequencies.

There has been a considerable effort done on the study of the influence of the equalizers depth on the overall performance of a read-channel. This also enforced the need for the development of low power continuous-time adaptive equalizers alternative to the FIR approach usually used with DFE.

An elegant solution comprising these requirements with PR4 coding was first proposed by Kenney as a logical intersection between DFE and fixed-delay tree search algorithm in [5.1]. Multilevel decision feedback equalization (MDFE) was presented as a fine solution for low-power acquisition on saturation recording magnetic read-channels, especially alluring to portable computers.

MDFE was proposed by Kenney et al. [5.2] as a quasi-optimum implementation of a maximum-likelihood sequence detector for run-length-limited (1,7) encoded data. One interesting feature of DFE used in MDFE is the possibility to tune both filter sections. This is usually accomplished using LMS modified algorithms and can improve BER achieving S/N ratio equivalent to PR4 at user bit density exceeding 2.0.

The circuit includes a forward and a backward filter, and a slicer similar to other DFE-based systems, whereas featuring a low power continuous-time adaptive equalizer solution alternative to the digital FIR approach usually used with DFE read channels. Causal ISI is eliminated using an equalizing filter in the feedback loop, but with reduced weights of the feedback taps. It also suggests the development of a colourless allpass continuous-time filter solution for the realization of the forward equalizer with equivalent performance to a long tapped-delay FIR filter as the key block of MDFE. The forward filter can be made adaptive for improved performance using a feedback LMS block.

5.2 Forward equalizer design

In more recent years various systems based on Decision Feedback Equalization (DFE) [5.1][5.3][5.4] have been reported for magnetic head read channels. DFE systems using digital FIR filter techniques have been able to meet the increase of data acquisition rates but at the expense of complexity and power dissipation. More recently, however,

low end drives have prompted considerable efforts [5.2][5.5][5.6] for developing a low power continuous-time adaptive forward equalizer alternative to the FIR approach. We present a comparative study of two such continuous-time adaptive equalizers designed to work with a sampling frequency of 100MHz which consume approximately 3mW at 3.3V supply voltage. This is less than one tenth of traditional FIR power needs, and practically independent of the sampling-frequency at the input of the slicer.

The theoretical prelude for the design of the architecture was studied by McEwen *et al*. in [5.7], where a taped delay FIR filter equalizer with varying depth was used to implement the forward equalizer in MDFE's architecture. This is a study on the optimized pole frequency that yields the local optima for a continuous-time second order and for a continuous-time third order equivalents to a long taped delay FIR filter.

5.3 Read-head pulse shape

The read head response model considered was the Lorentzian model given by

$$s(t) = \frac{1}{(1+(2t/\ pw50)^2)} \tag{5.1}$$

This proves to be a good model for the read-head as can be seen when compared with measured data from a real hard disk drive. The waveform is normalized to unitary peak amplitude and to pulse width *pw50=2T*, the time axis is normalized to *0.1T*.

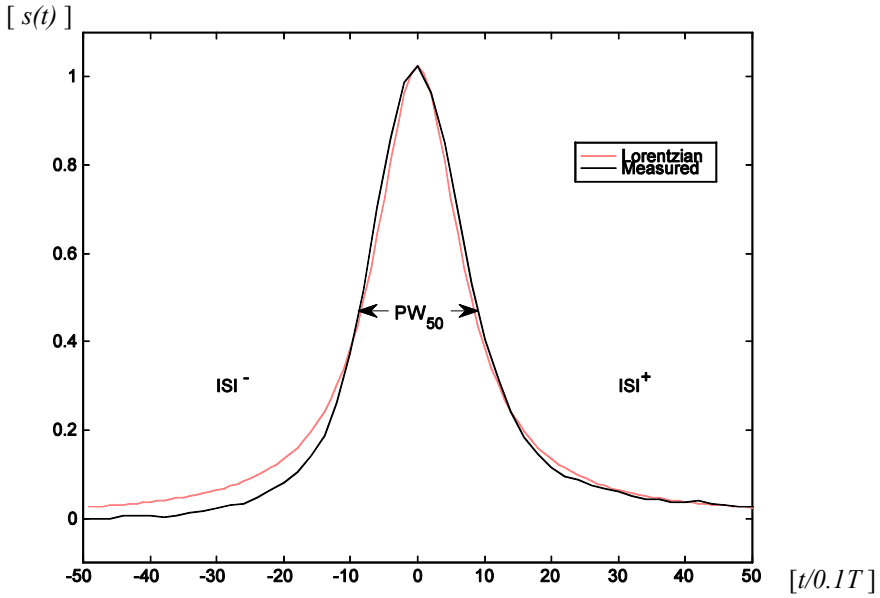

Fig. 5.1 – Impulse response versus Lorentzian Model.

5.4 Channel architecture and equalizer design

MDFE read channels basically consist of two equalizing filters and a decision element *(slicer),* as shown in the block diagram of Fig. 5.2. The forward equalizer is used for *precursor* ISI cancellation while the backward equalizer is a non linear *post cursor* ISI remover. It is of considerable interest that both filters operate in current-mode so that the outputs of these filters are added in the current summing node that precedes the sampling switch. The adaptation process depends on the generation of the error signal estimated by the difference between the prediction value at the input of the slicer and the data decision at its output.

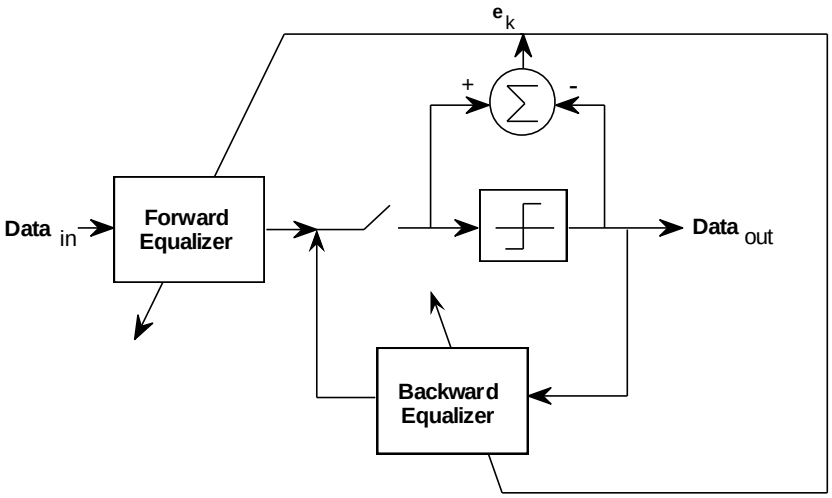

Fig. 5.2 – Block diagram of MDFE read-head channel.

This thesis is concerned with the design of the forward equalizer for a 100MHz sampling frequency, the following *a priori* pole location are derived from [5.7]:

$$\begin{aligned} &\text{Real Pole} && f = 8\ \text{MHz} \\ &\text{Complex Poles} && f_0 = 26\ \text{MHz} \quad Q = 0.6 \end{aligned} \tag{5.2}$$

Corresponding to the following Argand plot representation for the allpass forward equalizer

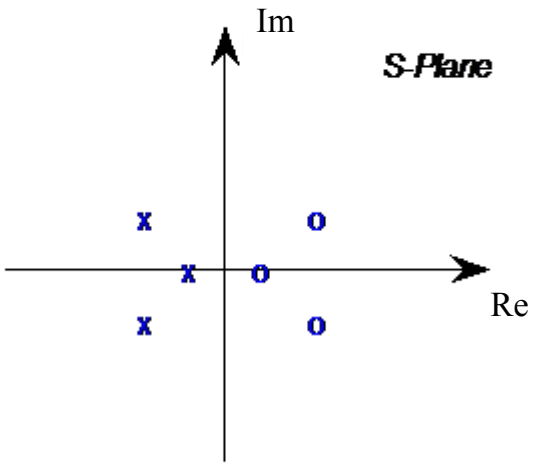

Fig. 5.3 – S-plane representation of ideal a priori pole locations.

The corresponding system transfer function can be expressed by

$$H(s) = \frac{-s^3 + 3.26 \cdot 10^8 s^2 - 4.1308 \cdot 10^{16} s + 1.3754 \cdot 10^{24}}{s^3 + 3.26 \cdot 10^8 s^2 + 4.1308 \cdot 10^{16} s + 1.3754 \cdot 10^{24}} \quad . \tag{5.3}$$

5.5 *Adaptive gm-C architectures*

For the above specifications, two *gm*-C current-mode structures were designed and compared based on transistor level simulations. Both architectures adapt using LMS modified algorithms [5.8], and allow the parasitic input capacitance in the *gm*s to be taken into account for very high frequency operation. The automatic tuning of the poles frequency also compensates process tolerances that influence the effective value of the active devices and capacitors. The equalizers linearity is mainly determined by the linearity of the transconductors and integrating capacitors. The DC voltage inherent to the simulated structures biases these transistors well beyond their threshold voltage for enhanced linearity behavior.

5.6 Canonical structure

Firstly, we considered the canonical structure illustrated in Fig. 5.4. It is composed of four equal value pseudo-differential transconductors embedded in a grounded capacitive network connected in a companion form state-space filter configuration.

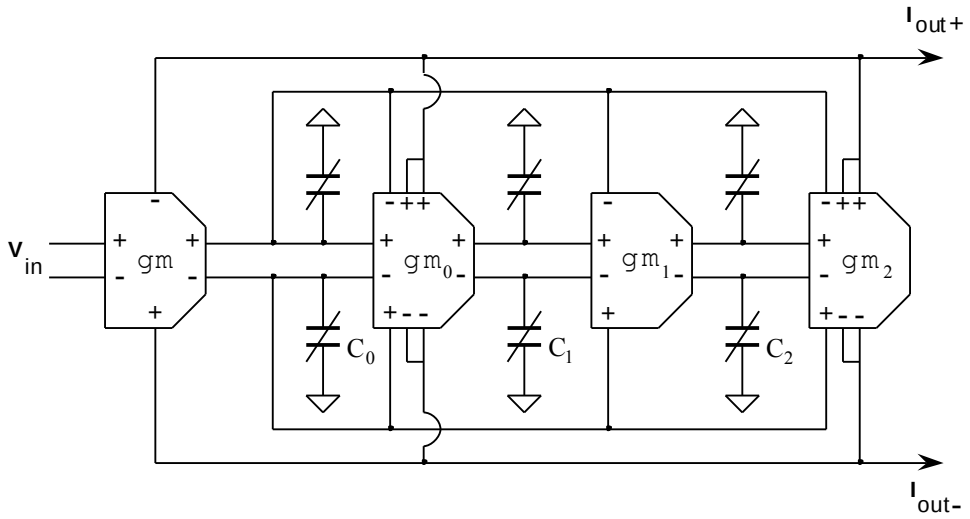

Fig. 5.4 – Canonical structure.

The corresponding 3rd order state-space system can be expressed as

$$\begin{cases} \dot{[i]} = [A]\cdot[i] + [B]\cdot i_{in} \\ i_{out} = [C]^T \cdot [i] + D \cdot i_{in} \end{cases} \tag{5.4}$$

where the system matrices are given by

$$[A] = \begin{bmatrix} -gm_0/C_0 & -gm_0/C_0 & -gm_0/C_0 \\ gm_1/C_1 & 0 & 0 \\ 0 & gm_2/C_2 & 0 \end{bmatrix} \tag{5.5}$$

$$[B] = \begin{bmatrix} gm_0/C_0 \\ 0 \\ 0 \end{bmatrix} \tag{5.6}$$

$$[C] = \begin{bmatrix} 2 \\ 0 \\ 2 \end{bmatrix} \tag{5.7}$$

$$D = -1 \tag{5.8}$$

Notice that matrix [A] assumes the typical *row-shape* characteristic of a companion form realization of the state-space model. The system transfer function is given by

$$H(s) = C^T \cdot (sI - A)^{-1} \cdot B + D \,. \tag{5.9}$$

Considering $gm = gm_0 = gm_1 = gm_2$ we obtain

$$H(s) = \frac{-s^3 C_0 C_1 C_2 + s^2 C_1 C_2 gm - s C_2 gm^2 + gm^3}{s^3 C_0 C_1 C_2 + s^2 C_1 C_2 gm + s C_2 gm^2 + gm^3} \,. \tag{5.10}$$

For equal-valued transconductors with a nominal transconductance value of 60μS, we obtain the following nominal values for the integrating capacitors, after subtracting the effect of the parasitic input capacitance of the *gm*s

$$C_0 = 0.083\ pF,\ C_1 = 0.43\ pF,\ C_2 = 1.77\ pF \,. \tag{5.11}$$

5.7 Orthonormal structure

As an alternative to the canonical structure described before we also considered the orthonormal structure represented in Fig. 5.5. Although the design of the orthonormal structure is usually a more complex approach, it can take a rather simplified format for the allpass filter. Moreover, it uses only one of the state variables to build the allpass current output signal (see matrix C in (5.14)) and thus making it more immune to mis-match and offset problems than the previous canonical structure.

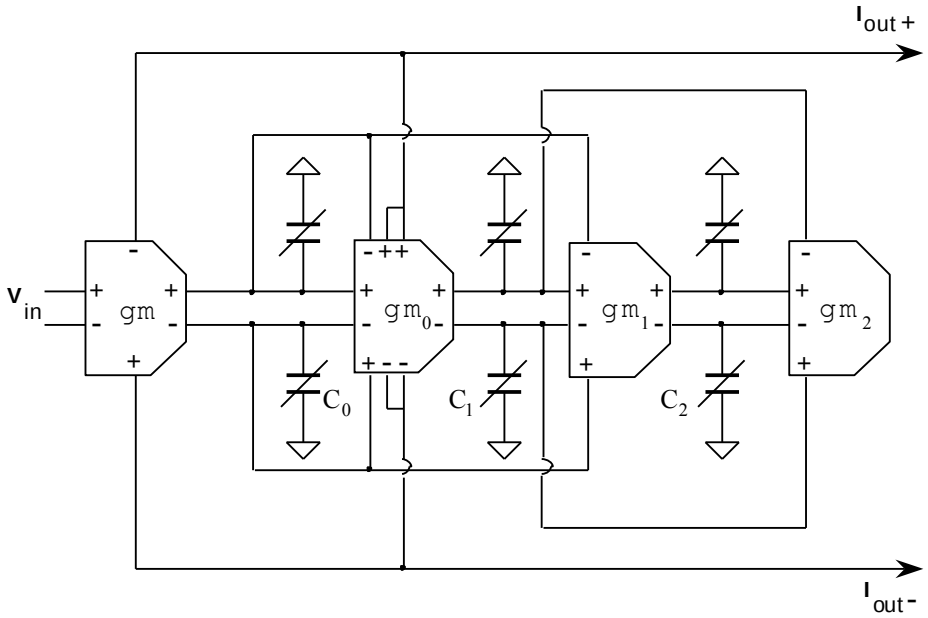

Fig. 5.5 – Orthonormal structure.

The corresponding 3rd order state-space system is also expressed by matrix equation (5.4) but the system matrices are now given by

$$[A]=\begin{bmatrix} -gm_0/C_0 & -gm_0/C_0 & 0 \\ gm_1/C_1 & 0 & -gm_1/C_1 \\ 0 & gm_2/C_2 & 0 \end{bmatrix} \tag{5.12}$$

$$[B]=\begin{bmatrix} gm_0/C_0 \\ 0 \\ 0 \end{bmatrix} \tag{5.13}$$

$$[C]=\begin{bmatrix} 2 \\ 0 \\ 0 \end{bmatrix} \tag{5.14}$$

$$D=-1 \tag{5.15}$$

A simple scaling of the system state-variables would transform it in the orthonormal ladder structure proposed in [5.9]. Hence, since the filter satisfies Lyapunov's equation

$$AK + KA^T + 2\pi bb^T = 0 \tag{5.16}$$

all the system state-variables are orthogonal and the dynamic range is optimized. The system transfer function for the structure in Fig. 5.5 is given by

$$H(s) = \frac{-s^3 C_0 C_1 C_2 + s^2 C_1 C_2 gm - s(C_0 + C_2)gm^2 + gm^3}{s^3 C_0 C_1 C_2 + s^2 C_1 C_2 gm + s(C_0 + C_2)gm^2 + gm^3} \tag{5.17}$$

Considering again equal-valued transconductors with the same nominal value of 60μS and subtracting the effect of the input capacitance of the *gm*s we obtain the following nominal values for the integrating capacitors

$$C_0 = 0.102\ pF,\ C_1 = 0.45\ pF,\ C_2 = 1.77\ pF\ . \tag{5.18}$$

The complete filter structure has been integrated in a 0.5μm digital CMOS technology. The transconductors are Pseudo-differential balanced transconductors and capacitors are formed by transistor-based structures consisting of arrays of unit size cells of 12.5fF. The nominal transconductance value is 60μS and the capacitance values are:

C_0=0.185pF, C_1=0.47pF, C_2=1.8pF (Canonical)

C_0=0.202pF, C_1=0.49pF, C_2=1.8pF (Orthonormal)

Features

- The parasitic capacitance in the *gm*s should be taken into account in the layout design and be subtracted from C_i thus allowing the transconductors to work at very high frequency.
- Automatic tuning of the frequency of the poles can compensate process tolerances that influence the effective value of the active devices (namely *gm*s) and capacitors.
- *gm*-C filters use transconductors, which are not generic blocks and had to be designed at device level.

- Note that the linearity of the filter is mainly determined by the linearity of the transconductors and of the integrating capacitors.

A simpler equivalent companion form 2nd order system was also designed and simulated, also featuring very high frequency, low power consumption and low supply voltage using adaptive state-space recursive filters based on current-mode *gm*-C structures. The pole locations for a two pole solution is also obtained from McEwen *et al*. [5.7]

$$\text{Complex Poles} \quad f_0 = 26.4\ \text{MHz} \quad Q = 0.66\ . \tag{5.19}$$

The filter operates in current-mode so that the outputs are added in the current summing node that precedes the sampling switch. The state-space system is expressed by matrix equation

$$\begin{cases} \dot{[i]} = [A]\cdot[i] + [B]\cdot i_{in} \\ i_{out} = [C]^T \cdot [i] + D \cdot i_{in} \end{cases} \tag{5.20}$$

where the system matrices corresponding to the proposed *gm*-C filter topology for this 2rd order forward equalizer are given by

$$[A] = \begin{bmatrix} -gm_0/C_0 & -gm_0/C_0 \\ gm_1/C_1 & 0 \end{bmatrix} \tag{5.21}$$

$$[B] = \begin{bmatrix} gm_0/C_0 \\ 0 \end{bmatrix} \tag{5.22}$$

$$[C] = \begin{bmatrix} 0 \\ 2 \end{bmatrix} \tag{5.23}$$

$$D = -1 \tag{5.24}$$

and hence the allpass system transfer function is given by

$$H(s) = \frac{s^2 C_0 C_1 - s C_1 gm + gm^2}{s^2 C_0 C_1 + s C_1 gm + gm^2} \tag{5.25}$$

Considering equal-valued transconductors with a nominal value of 60μS we used the following nominal values for the integrating capacitors, matching the theoretical work [5.7] for the ideal pole locations of the forward equalizer

C_0=0.22pF, C_1=0.60pF (2^{nd} order)

5.8 Adaptive capacitor array

The variable capacitors are implemented using polarized MOSFET capacitor arrays used as integrating capacitors. The adaptation of the *gm*-C filters previously described is achieved by means of integrating capacitor structures C_i consisting of a constant *course* MOSFET capacitor C_i' in parallel with an N-bit digitally controlled *fine* tuning capacitor array ΔC_i, as shown in Fig. 5.6.

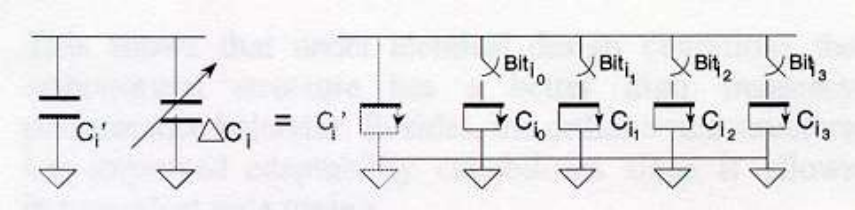

Fig. 5.6 – Integrating capacitors are formed by a fixed capacitor in parallel with a digitally controlled capacitor-array.

the total integrating capacitance is given by

$$C_i = C_i' + \Delta C_i \tag{5.26}$$

where

$$\Delta C_i = \sum_{k=0}^{N-1} C_{ik} \cdot Bit_{ik} \tag{5.27}$$

and

$$C_{ik} = 2^k \cdot C_{i0} \tag{5.28}$$

where C_{i0} =12.5fF is the nominal unit size capacitance value, and thus (5.27) can be expressed as

$$\Delta C_i = C_{i0} \cdot \sum_{k=0}^{N-1} 2^k \cdot Bit_{ik} \qquad (5.29)$$

The minimum value C_i' and the maximum value $C_i' + max(\Delta C_i)$ of each integrating capacitor C_i are dimensioned to allow the desirable placement of the poles, even under worst case process tolerances that influence the actual value of *gm*s and of the integrating capacitors. The number of adaptation bits must provide sufficient adaptation precision of the arrays without unduly increasing the circuit complexity. For both structures described before we considered N = 4-bit capacitor arrays made of biased 12.5fF unit size transistor cells that can be switched on and off by the adaptive control logic. The adaptation process is assumed to be done during the clock recovery preamble and be stable at the decision instants. Alternatively the capacitor array can be loaded in parallel and subsequently adapted to optimum values.

5.9 Transconductors

The transconductors employed in the above filters are based on balanced pseudo-differential lossy-C structures, as shown in Fig. 5.7. Unlike in the circuit used in [5.10], biasing is provided by the feedback loops established in the filter, yielding improved stability and noise immunity. Moreover, the transistors dimensions determining the biasing voltages were calculated to minimize the allowed mismatch while maintaining maximum frequency performance. Computer simulations show that such transconductors are capable of maintaining the correct operation of the filter for supply voltages as low as 1.8 V.

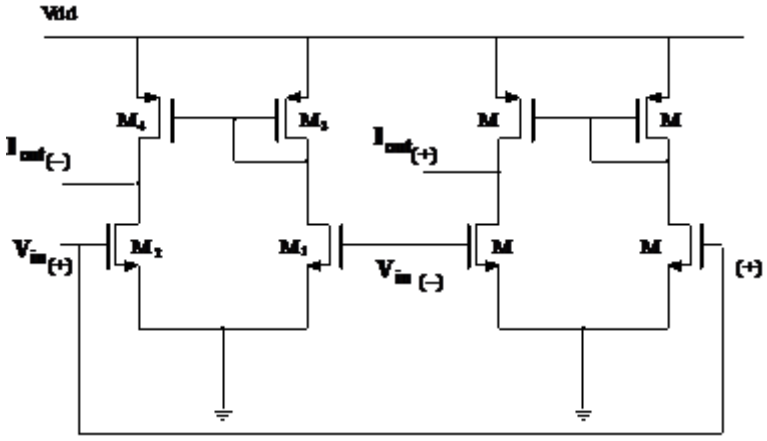

Fig. 5.7 – Balanced pseudo-differential transconductor.

The transconductors are low-mismatch high bandwidth balanced pseudo-differential transconductance cells proposed in [5.14]. The nominal transconductance value was designed to set the size and values of the integrating capacitors in a usable range in a solid state IC, whilst obtaining very low power consumption working at very high frequency. This also implied avoiding the increase of die area due to big capacitor values (e.g. for C_2) and avoiding small capacitor values (e.g. for C_0) from getting to close to the parasitic capacitance of the transconductor cell.

The DC voltage inherent to the simulated structures biases these transistors well beyond their threshold voltage for enhanced linearity behavior.

5.10 Results and discussion

Frequency response

Transistor level simulations of both 3rd order structures with nominal integrating capacitance values produced the amplitude and phase versus frequency response characteristics shown in Fig. 5.8 and Fig. 5.9, respectively for the canonical and orthonormal structures.

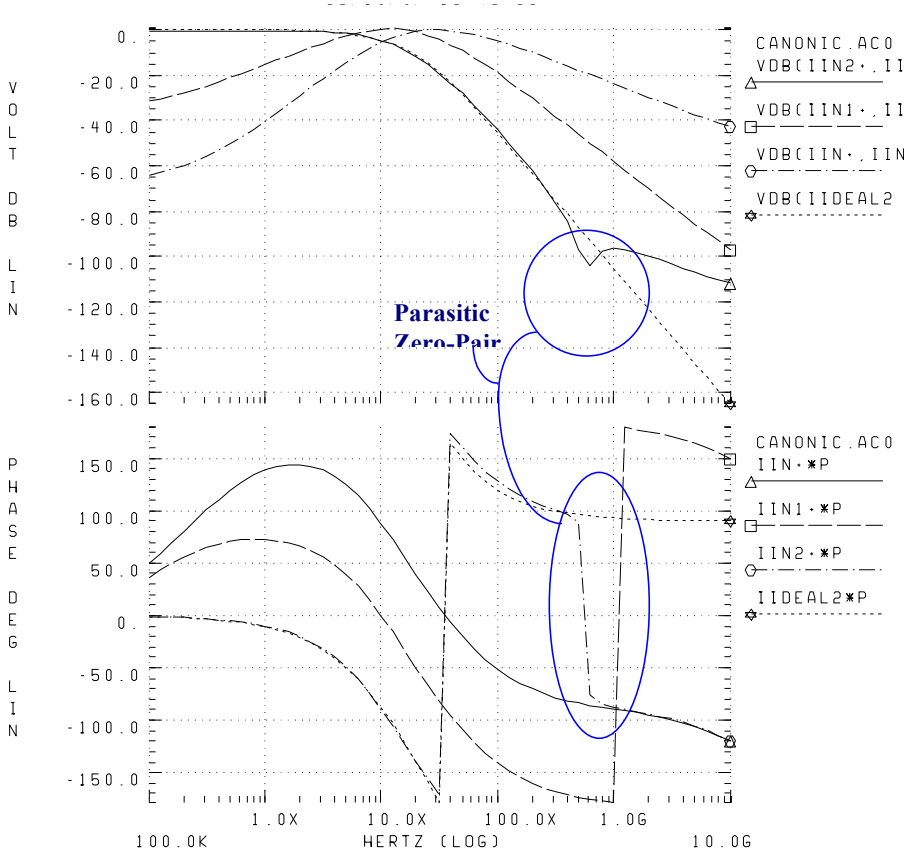

Fig. 5.8 – Frequency response of the canonical filter structure, for nominal integrating capacitance values.

For the canonical equalizer, the behavior of state variables I_{In_0} and I_{In_1} is close to ideal, but there is a parasitic zero-pair mismatch in state variable I_{In_2} around 450MHz. This error does not affect significantly the time response of the filter. In the orthonormal structure all state variables I_{In_i} nearly match the ideal I_{Ideal_i} amplitude and phase characteristics well over 1GHz.

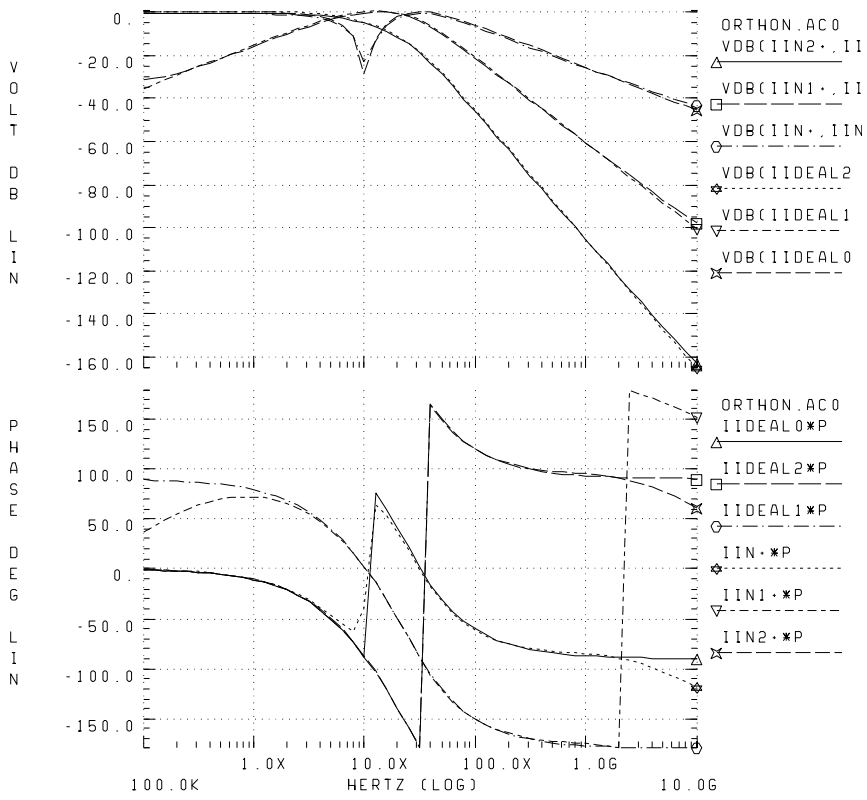

Fig. 5.9 – Frequency response of the orthonormal filter structure, for nominal integrating capacitance values.

This shows that under identical design conditions the orthonormal structure has a better high frequency performance behavior. Besides, the orthonormal structure has improved adaptability capabilities since it allows independent pole tuning.

Transient response

Transistor level AC simulations of both 2nd order and 3rd order allpass equalizers with nominal integrating capacitance values closely match the ideal amplitude and phase characteristics of the allpass filters up to 1GHz. The corresponding transient responses to a dibit input was simulated using measured data from a magnetic read head for two consecutive flux transitions with ISI. Fig. 5.10 depicts the equalized transient response of the second order filter and of the third order canonical filter. The differential output closely

matches the ideally predicted values, hence the results are nearly superimposed with the ideal response of each of the two equalizers. The simulated power consumption for the 3rd order is 3mW and the power consumption for the 2nd order equalizer is 2mW, whereas both equalizers have a total die area of less than 0.1mm^2.

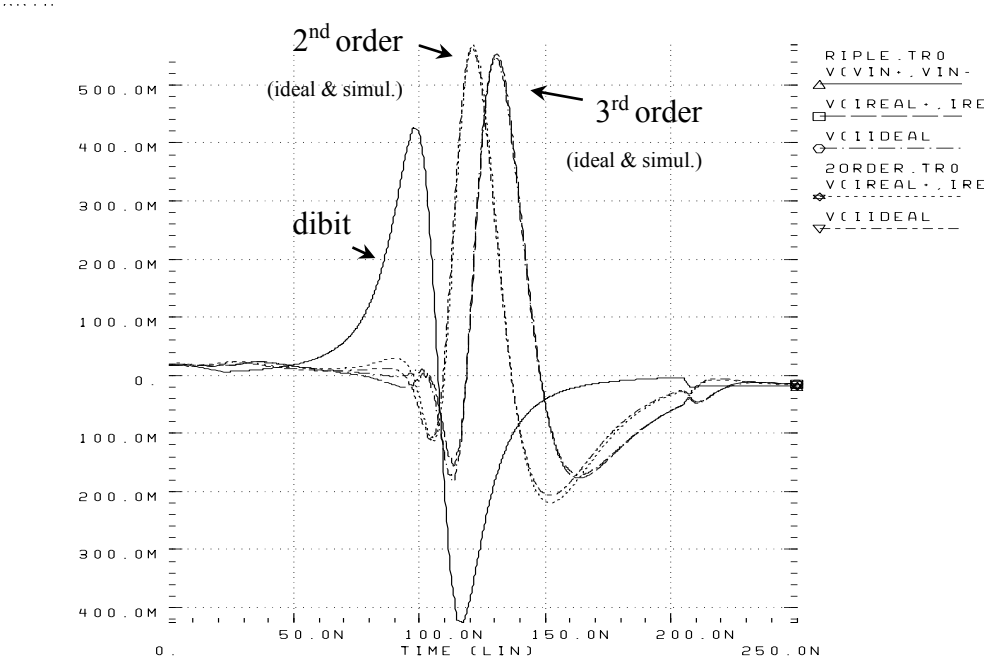

Fig. 5.10 – Dibit-response of the 2nd order and 3rd order allpass equalizers.

For the 3rd order equalizers, the transient response of both structures was analyzed using an input corresponding to measured data[42] from the magnetic read head. This waveshape V_{in} represents consecutive transitions, one up and one down, usually mentioned as *dibit* response. The resulting equalized transient response of the orthonormal and canonical outputs are superimposed and are both represented by I_{real} in Fig. 5.11, showing that both structures practically match the predicted response from the ideal implementation I_{Ideal}.

[42] Courtesy of IBM.

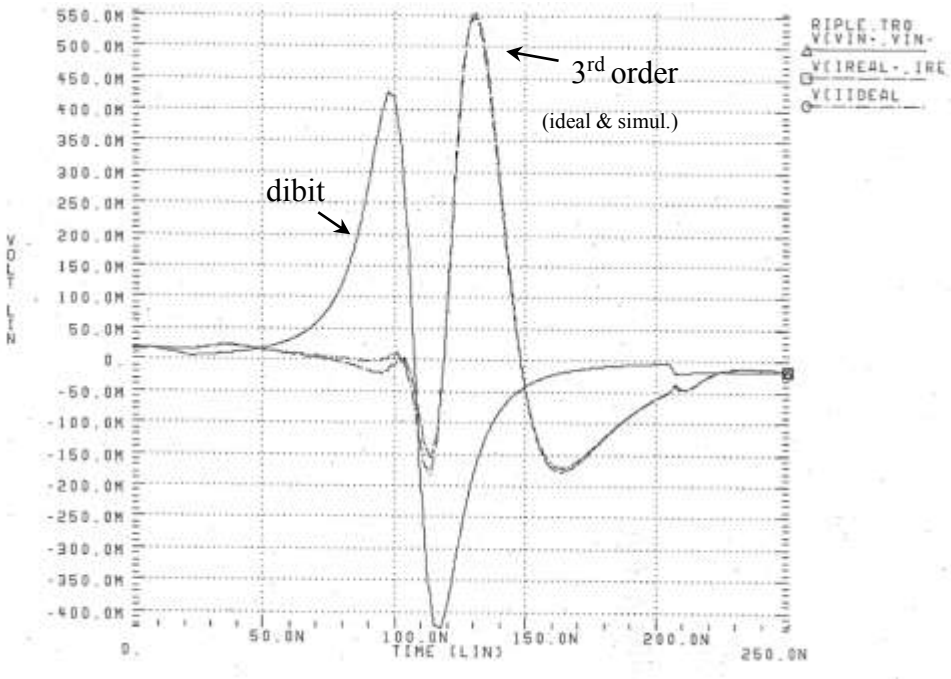

Fig. 5.11 – Dibit-response of the Allpass Filter.

The layout of the 3rd order orthonormal active circuitry of the equalizers is depicted in Fig. 5.12, including the twelve control bits (four for each integrating capacitor) and the transconductor cells and capacitor arrays. This layout also includes capacitors C_i' for a total active area of 200μm x 300μm. Table 5.1 shows the main electrical characteristics of the 3rd order allpass filters.

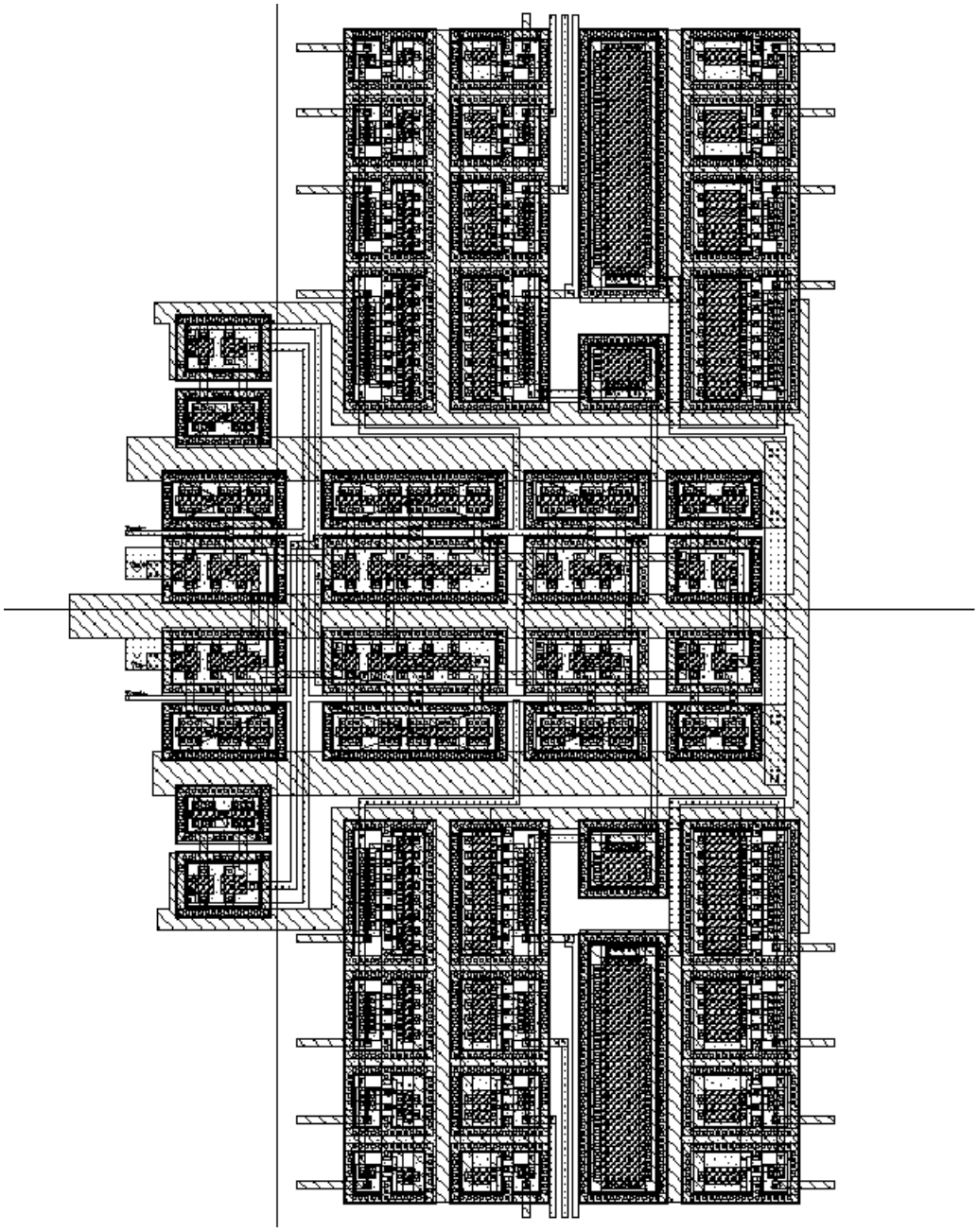

Fig. 5.12 – Layout of active circuitry.

Table 5.1 – Main characteristics of the allpass filter.

Technology	0.5μm Digital CMOS	
Poles Frequency	8 to 26	MHz
CMRR	80	dB
PSRR, GSRR	60	dB
THD	–50	DB
Power supply	3.3	V
Power dissipation	3.5	mW
# Active devices	50	
Active area	0.2x0.3	mm^2

We present a comparative study of two continuous-time equalizers for MDFE read channels. They can both operate with supply voltages as low as 1.8 V while reducing consumption by a factor of 10 to 100, compared to conventional FIR digital equalizers exhibiting equivalent performance. Besides its improved adaptability, the orthonormal structure shows improved frequency response over the canonical structure and hence suggests that the orthonormal structure is a better realization of the allpass forward equalizer, especially at higher data rates.

Conventional DFE uses a FIR filter as a forward equalizer to cancel the non-causal precursor ISI, however [5.7] suggests that an adaptive analog implementation can show equivalent performance to that of a long (24 taps) FIR filter, whilst reducing power consumption. In this work we propose and show simulation results for a 2^{nd} order and for a 3^{rd} order allpass continuous-time filter, both capable of implementing the adaptive forward equalizer.

Table 5.2 comprises several equalizers proposed for implementation the forward equalizer in PRML and DFE read channels.

Table 5.2 – Equalizer evolution.

Year	Technology			Freq./Data rate	Power	Area
1994	1.2μm CMOS	[5.11]	SC-FIR	100 MHz	900 mW	44 mm^2
1995	0.8μm CMOS	[5.12]	A-FIR	240 MHz	426 mW	2.9 mm^2
1996	0.6μm CMOS	[5.13]	SC-FIR	200 MHz	507 mW	13 mm^2
1997	0.5μm CMOS	[5.14]	*gm*-C	100 MHz	3 mW	0.06 mm^2
1997	0.6μm CMOS	[5.15]	*gm*-C	150 Mb/s	90 mW	0.8 mm^2
1998	0.25μm CMOS	[5.16]	A-FIR	360 Mb/s	21 mW	–
1999	1.0μm CMOS	[5.17]	A-FIR	80 Mb/s	280 mW	6.7 mm^2
2002	0.5μm CMOS	[5.18]	A-FIR	100 Mb/s	130 mW	1.3 mm^2
2005	0.18μm CMOS	[5.19]	*gm*-C	70 MHz	21.8 mW	–
2007	0.18μm CMOS	[5.20]	*gm*-C	160 MHz	15 mW	–
2008	0.18μm CMOS	[5.21]	*gm*-C	400 MHz	80 mW	–

5.11 Least mean squares algorithm

The most common adaptation algorithm for adaptive equalizers is the least mean squares algorithm (LMS) [5.8][5.22]. The simplest of the adaptive solutions for channel equalization, would essentially use the sign of the state variables i_1, i_2 and i_3 of the state space filter instead of sign of the term given by the expression derived from the LMS algorithm.

This was proposed and demonstrated to converge by Kenney for the allpass equalizer.

5.12 Tuning schemes

Master-slave filter tuning

For the implementation of the MDFE equalizers, two techniques where considered for the adaption coefficients. The most common are the LMS-based algorithms, however these generally imply the usage of additional filters, continuously working at high frequency, with similar complexity to the equalizer filter.

Another common topology used to tune active filters, especially useful in bandpass filters, is the master-slave technique. With these scheme, a PLL is usually used to lock the operating frequency of a control (master) oscillator to the operation of a second (slave) filter using similar basic blocks (e.g. integrators, transconductors, passive components). This way, the process variation of these basic blocks can be canceled and the desired frequency for the filter can be determined in respect to the oscillator parameters.

An alternative to an LMS-based algorithm for the adaptation process is to run a tuning command to calibrate the equalizer. This can be issued once at setup, to allow the compensation of transconductor and capacitor process variations from nominal values, hence, the time constants for the desired target of the equalizing filter can be set independently of process variations. A bandgap voltage reference can be used to control a simple slave filter together with a successive approach register (SAR) to allow the setting of the time constant. Using similar devices in the equalizer sets the pole/zero frequencies independently of process variations, temperature and supply voltage, to the nominal desired values.

This technique was implemented with success on an active OPAMP-RC filter *txumtspci* designed in 2000 at Chipidea using ATMEL/at57500 process for an UMTS transmit channel capable of tuning the filter time constant.

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Chapter 6

Design and evaluation of application circuits

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6.1 Introduction

This chapter presents measured and simulation results of application circuits developed to demonstrate the studied solutions.

Firstly we present a servo burst area demodulator for magnetic disk drives. This design was applied in the AT78C1000 servo controller integrated circuit proposed for a portable magnetic disk drive system. This chip was designed and fabricated using ATMEL's at55000 process in Colorado Springs CO in 1999. The IC is a dual voltage 128 pin TQFP mixed signal 0.5μm standard digital CMOS technology.

In this solution, the area integrator block consists of a continuous-time first order one pole $1/s$ integrating filter, implemented using a *gm*-C filter topology. The integrator is realized using a pseudo-differential balanced transconductor and of a MOSFET bank array to implement a variable gain integrating capacitor, ranging from approximately 1pF to 64pF to allow large operability, either in the number and width (and data rate) of the usable servo burst sectors — A, B, C, D.

We also designed two ICs to test the equalizer filters, MDFE–AP02 using ES2/ECDM05 technology, and MDFE-AP04 using technologies ATMEL/ECDM06 and ATMEL/at55000. This chip also includes the auto-biased transconductor cell described in chapter 5.

Finally, we tested a tuned filter strategy based on a bandgap voltage reference combined with a *Master-Slave* filter. This was implemented in integrated circuit *txumtspci* designed using ATMEL/at57500 mixed signal 0.18μm process, and we were able to test a tuning scheme topology for an UMTS transmit channel capable of setting the time constant C/gm of a tunable filter. This technique allows that the filter coefficients become independent of the process variation of capacitor and transconductor values, whilst becoming temperature and supply voltage independent.

The bandgap reference was designed and tested in ES2 Rousset's facilities and integrated in the analog library cell foundry kit under name BG004.

6.2 *An application example to servo demodulation (AT78C1000)*

Servo information is essential to control the positioning of the actuator exactly on track and precisely regulate the rotation speed of the spindle. The classic servo controller functionality requires both analog and digital circuitry and can be implemented in a single slave IC device or integrated with other disk drive functions to respond to basic requests from the host digital signal processor (DSP). For these tasks it is usually assisted by external circuitry (e.g. ADC, DAC, Frequency Synthesizer, and Precision Voltage Reference).

Whereas mass storage multi-disk hard drives formerly provided a separate platter surface just for servo using dedicated head and pulse detector channel, much cheaper single disk drives with embedded servo provide all necessary servo demodulation information in servo designated sectors, as shown in Fig. 6.1.

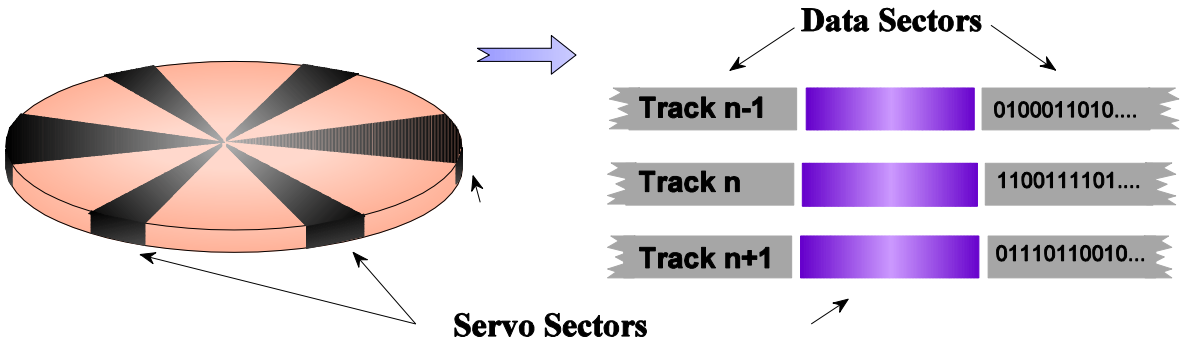

Fig. 6.1 – Servo sectors in the hard disk.

These servo sectors are evenly distrusted along the disks surface, interleaved with data sectors, in such a way that practically constant monitoring of the read head positioning is assured, without unduly decreasing usable space and data transfer speed.

The servo sector information format depends on the manufacturer, but typically consists of three data fields with special characteristics: *Preamble, Gray Code, and Servo Bursts – A, B, C, D,* as shown in Fig. 6.2.

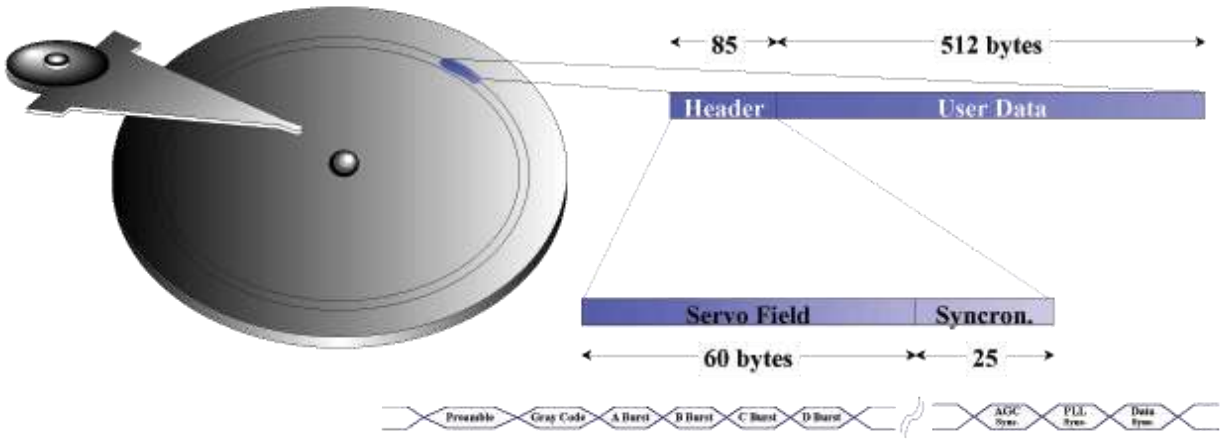

Fig. 6.2 – Servo sector information format.

- The ***Preamble*** field usually consists of alternate positive and negative pulses that can be used during automatic gain control (AGC) to calibrate a variable gain amplifier (VGA), and during the synchronization lock[43] of a PLL block, for most servo demodulators still rely on synchronous detection for high data integrity. This field contains the servo field ID that is used to confirm that the magnetic head is in the desired servo field sector.
- The ***Gray Code*** field usually contains several identification bytes concerning head positioning and manufacturer specific reserved data, such as: track ID, general purpose ID, servo ID and head ID. This data, usually encoded as RLL (1, 3)[44] Gray code, is acquired and decoded in servo mode and subsequently transmitted to the interface microcontroller. The usage of Gray coded or raw binary data in this field is optional

[43] The length of this field can be programmed and the usage of a zero phase start PLO typically reduces the number of required cycles, hence providing roughly ineffectual time overhead.

[44] The advantages of using this scheme are the low ratio (2:1) between usable high and low frequencies and the more efficient use of lower servo format. For further explanation please consult *Run-Length Limited* (RLL) coding on page 56 of chapter 3.

and depends on the disk manufacturer. In fact, correct operation is attainable regardless of the information in this sub-field and hence some manufacturers simply choose not to include them to reduce complexity and data storage overhead.

- The ***Servo Bursts*** are specially written zones on the disk that are intentionally misaligned with the center of the track as shown in Fig. 6.3. Hence, the amplitude of the read signal is proportional to this misalignment, showing maximum peak-to-peak voltages when the head is exactly centered on track and minimum values when it is between two adjacent tracks. Typically four sub-fields are used: one exactly centered on track (*C*), one in-between tracks (*D*) and two symmetrically off centered (*A* and *B*), although once again, depending on the manufacturer [6.1], this field can have diverse formats. The controller estimates the position of the read head relatively to the center of the track by comparing the amplitudes of these bursts, e.g. by keeping the amplitudes of *A* and *B* equal or minimizing (*A* – *B*) or maximizing (*C* – *D*).

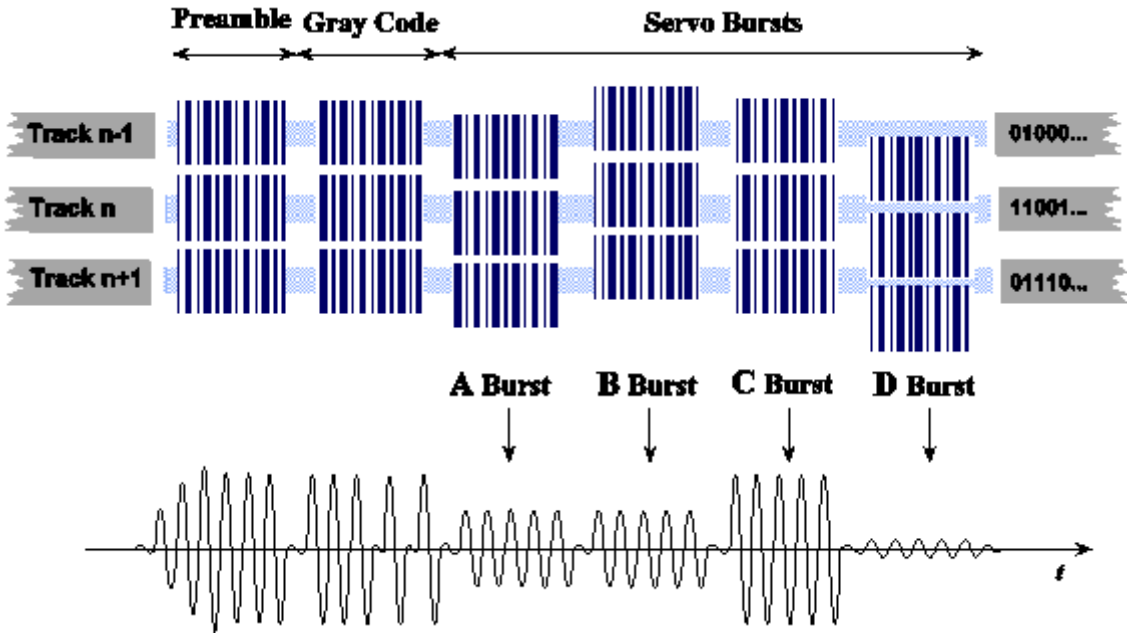

Fig. 6.3 – Servo bursts field format.

Off-track interference

Off-track interference occurs when the read head is not exactly on track, and hence, a bit from an adjacent track is sensed while reading a specific track on the disk. For high areal density the concentric tracks are packed together close to the value of linear density, thus high precision positioning is necessary to avoid off-track interference.

The preamble field, is used during automatic gain control and during the phase lock of the servo demodulation circuitry to the data stream so that the Gray code field may be read correctly. This field together with a servo mark (not shown in the diagram) asserts that the magnetic head is in the servo sector. While the track number is used to control the coarse position of the read head, the servo bursts confer its fine positioning on track. The linear signal produced by the processing of these bursts as the head moves off-track in either direction from the track center is sensed on the read head while reading these special misaligned bursts.

Considering (*A*) and (*B*) bursts, the amplitude of the read signal is proportional to this misalignment, showing equal peak-to-peak voltages when the head is exactly centered on track and minimum values when it is between two adjacent tracks.

The voltage values acquired in the read head during the read process of the servo bursts are roughly proportional (or inversely proportional) to the amount of offset from the head center to the track center, as is depicted in Fig. 6.4.

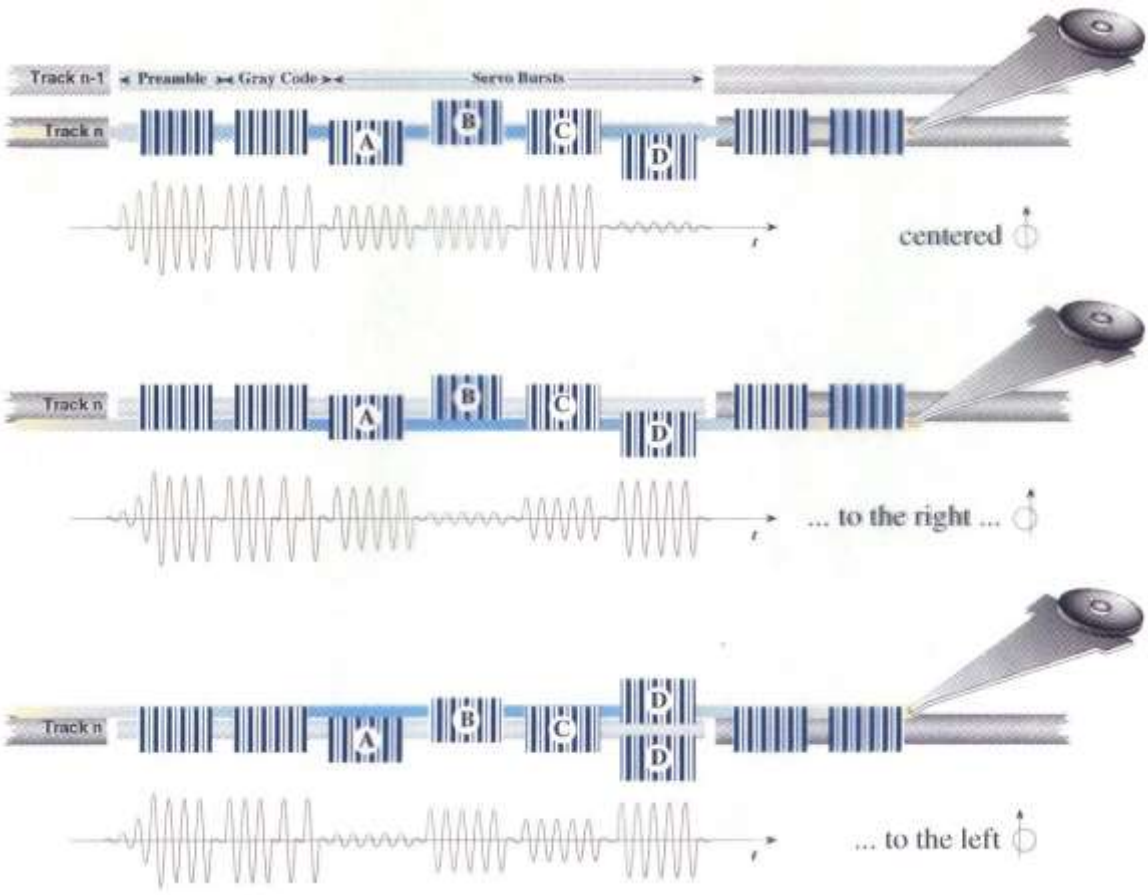

Fig. 6.4 – Offtrack interference.

This feedback control is dependent on accurate amplitude assessment and therefore an analog-to-digital converter is required. The servo demodulation channel usually works at less than half of the read channel data frequency and only during the servo field sector, hence, simplified architectures have been presented [6.4][6.5] that take advantage of time interleaving to share most of the blocks necessary for each of these channels, thus building read/write channels with integrated servo demodulation. The tendency to reach for minimum cost systems, especially important in low end products, makes this solution attractive and further pushes for completely integrated functionality in a single mixed signal IC, combining all referred auxiliary blocks, a digital processor and combined servo and data channels. The most common servo burst demodulation techniques: **peak-detection** and **area-detection** will be briefly described.

Peak detect servo burst demodulator

The peak detection architecture in Fig. 6.5 has been held up from the classic peak detection read channels and basically consists of an input variable gain amplifier (VGA), a continuous-time low-pass filter (LPF), an optional full-wave rectifier and a peak-detector circuit, followed by an analog to digital converter **(**ADC**).**

The peak-detection block is usually a clamper circuit whose analog output level is quantified at the sampling instants by the ADC and dispatched to the processor. Alternatively, a synchronization circuit can be used to sample the pulses at their peak voltages. Area demodulation can be obtained by replacing the peak-detection block by a continuous-time integrator.

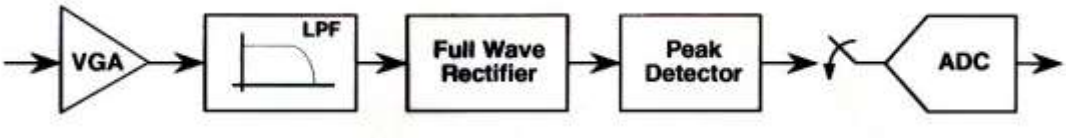

Fig. 6.5 – Peak detect servo burst demodulator architecture.

The purpose of the peak detection block is to hold the maximum voltage value during acquisition so that it can be sampled at the end of the burst, as is described in Fig. 6.6.

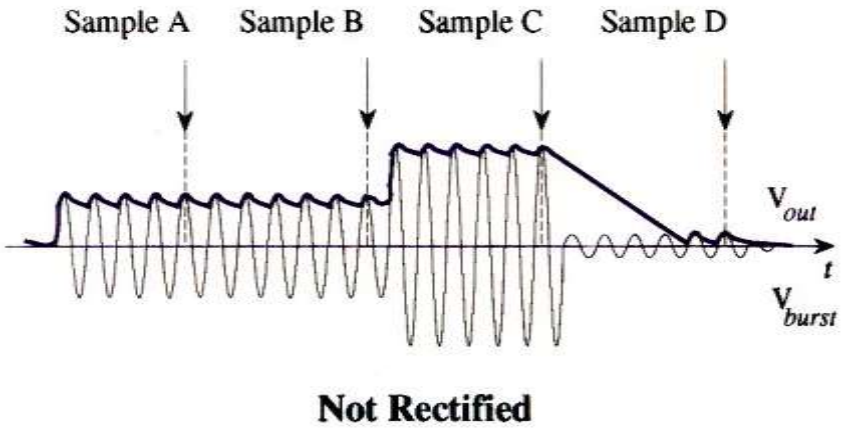

Fig. 6.6 – Peak detect servo burst demodulation waveforms.

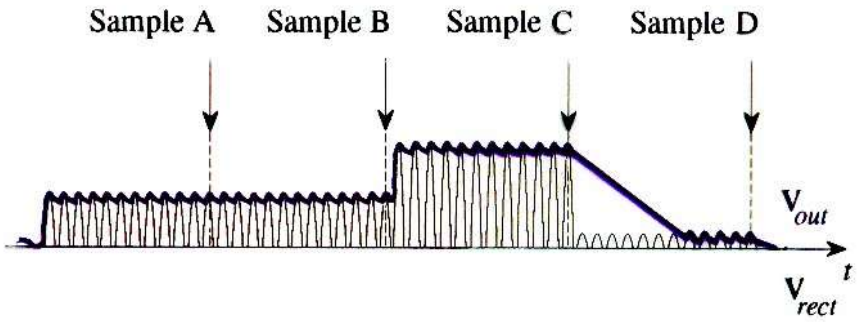

Fig. 6.7 – Rectified peak detect servo burst demodulation waveforms.

Averaging the contribution of several pulses eliminates the dependence of the sampled voltage on the shape of the last pulse and can easily be processed asynchronously. Moreover, the voltage sample is inherently held in the capacitor bank and subsequently acquired at a programmable instant near the end of each burst, as depicted in Fig. 6.9.

The analog output level is quantified at the sampling instants by the ADC and dispatched to the processor. The main advantages of this technique are simplicity and the small number of cycles required for each servo burst, however, the voltage value during sampling depends mostly on the shape of the last pulse and asynchronous acquisition can lead to some inaccuracy.

Area detect servo burst demodulator

The peak detection demodulator architecture has been held up from the classic peak detection read channels and basically contains an input VGA, a continuous-time low-pass filter, an optional rectifier block and a peak-detector circuit, followed by an analog to digital converter. The peak-detection block is usually a clamper circuit whose analog output level is quantified at the sampling instants by the ADC and dispatched to the processor. Alternatively, a synchronization circuit can be used to sample the pulses at their peak voltages. Area demodulation can be obtained by replacing the peak-detection block by a continuous-time integrator, as shown in Fig. 6.8.

Area integration to that multiplexer makes these diverse channels coherent

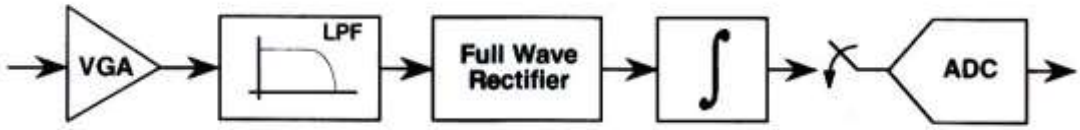

Fig. 6.8 – Area detect servo burst demodulator architecture.

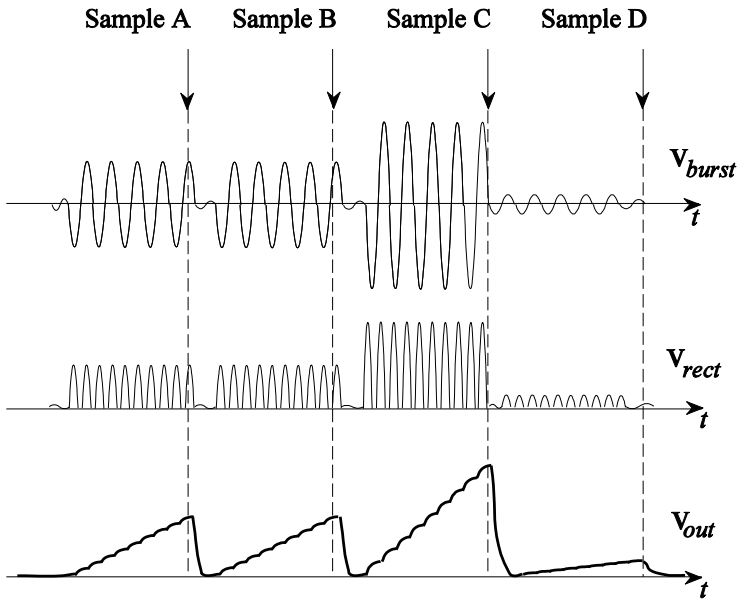

Fig. 6.9 – Area detect servo burst demodulation waveforms.

Averaging the contribution of several pulses eliminates the dependence of the sampled voltage on the shape of the last pulse and can easily be processed asynchronously. Moreover, the voltage sample is inherently held in the capacitor bank and subsequently acquired at a programmable instant near the end of each burst, as depicted in Fig. 6.9.

The schematic representation shown in Fig. 6.10, is one of the possible implementations of the integrator block in Fig. 6.8, and has been realized using auto-biased high frequency transconductances. The input *gm* converts voltage to current allowing the next stage to operate in current mode and the output feedback *gm*, implements a resistor of $1/(2 \cdot gm)$. The gain of the integrator is set by the capacitor array C_0 and the feedback path on gm_0 stabilizes the common mode voltage.

Continuous-time integrator

The programmable *gm*-C filter proposed for the implementation of the area integrator block is shown in Fig. 6.10. It is a fully balanced current-mode structure consisting of two transconductors and of a MOSFET capacitor bank array C_i. Transconductor gm_0 converts the input voltage to current, while capacitor array C_i and transconductor gm_1 realize the continuous-time integrator.

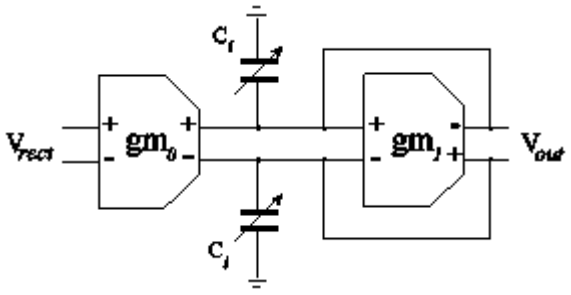

Fig. 6.10 – Area integrator implementation.

At design level, gm_0/gm_1 ratio establishes the nominal gain of the integrator and its power consumption. Likewise, programming C_i allows additional flexibility and accurate control of the integrated signal for a large range of operating frequencies and for a variable number of utilized burst cycles. The integrator schematics depicted in Fig. 6.11 embodies a high frequency auto-biased transconductor that uses current feedback to set the pole of the filter while stabilizing the common mode voltage, as described in [6.8]. The estimated area of the rectified pulse stream is assessed differentially at the current summing nodes I_{rect-} and I_{rect+}. Following the ADC acquisition, an auxiliary switch quickly resets the capacitor bank so that the next burst can be integrated

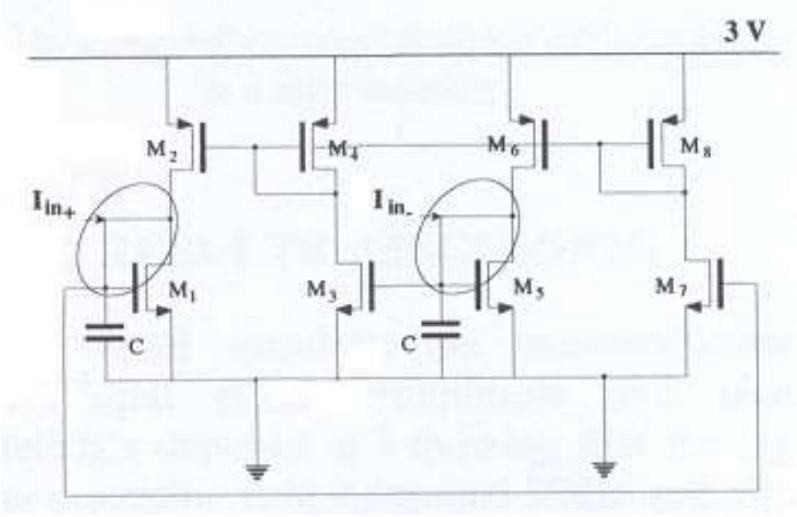

Fig. 6.11 – Area integrator core schematics.

Programmability and gain adjustment

The referred gain adjustment is performed by the integrating capacitor array C_i, as is similarly described in [6.13][6.14][6.15]. The DSP initially loads and subsequently adapts the capacitor array according to the feedback information given by the amplitudes of *A*, *B*, *C*, *D*. This tuning procedure also neutralizes deviations due to fabrication tolerances and occurs at lower speed to assure stability. The integrating capacitor C_i combines a binary weighted MOSFET array of 250fF unit size cells, connected in parallel and digitally controlled by MOS switches, as shown in Fig. 6.12. The transconductance value is 60mS and the capacitance values range is given by hexadecimal code in the digital bus.

Process tolerances that influence the effective value of the active devices and capacitors can be compensated by properly programming the capacitor structure of C_0 that consists of an 8-bit digitally controlled tuning capacitor array ΔC_0**,** as shown in Fig. 6.12.

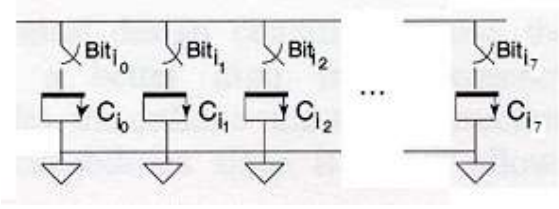

Fig. 6.12 – The integrating capacitor consists
of a digitally controlled capacitor-array.

An 8-bit structure provides sufficient precision and versatility at fairly low complexity overhead. The capacitance value is imposed by the hexadecimal vector in the digital bus and is given by

$$C_i = \sum_{k=0}^{7} C_k \cdot Bit_k \text{ , with } C_k = 2^k \cdot 250\text{fF} \tag{6.1}$$

Consequently, C_i can take any value in the range

$$\begin{aligned} C_{min} &= 0.250\text{pF} = 2^0 \cdot 250\text{fF} \quad (\text{code } 00\text{H}) \\ C_{max} &= 63.75\text{pF} = (2^8\text{-}1) \cdot 250\text{fF} \quad (\text{code FFH}) \end{aligned} \tag{6.2}$$

The operating frequency scope is hence larger than two decades and upper limited by the parasitic input capacitance of the transconductance cell. The self-imposed common mode voltage of the transconductances biases these transistors beyond their threshold voltage for enhanced linearity behavior.

Frequency response

Transistor level simulation of the area integrator circuit for integrating capacitance values of 10 pF to 40 pF, produce the amplitude and phase versus frequency response characteristics shown in Fig. 6.13. The plot of the integrated voltage between nodes I_{rect} and I_{rect+} indicate that the filter behaves as an integrator in the band of interest, showing a second pole near the *ft* of the transistors as described in [6.8].

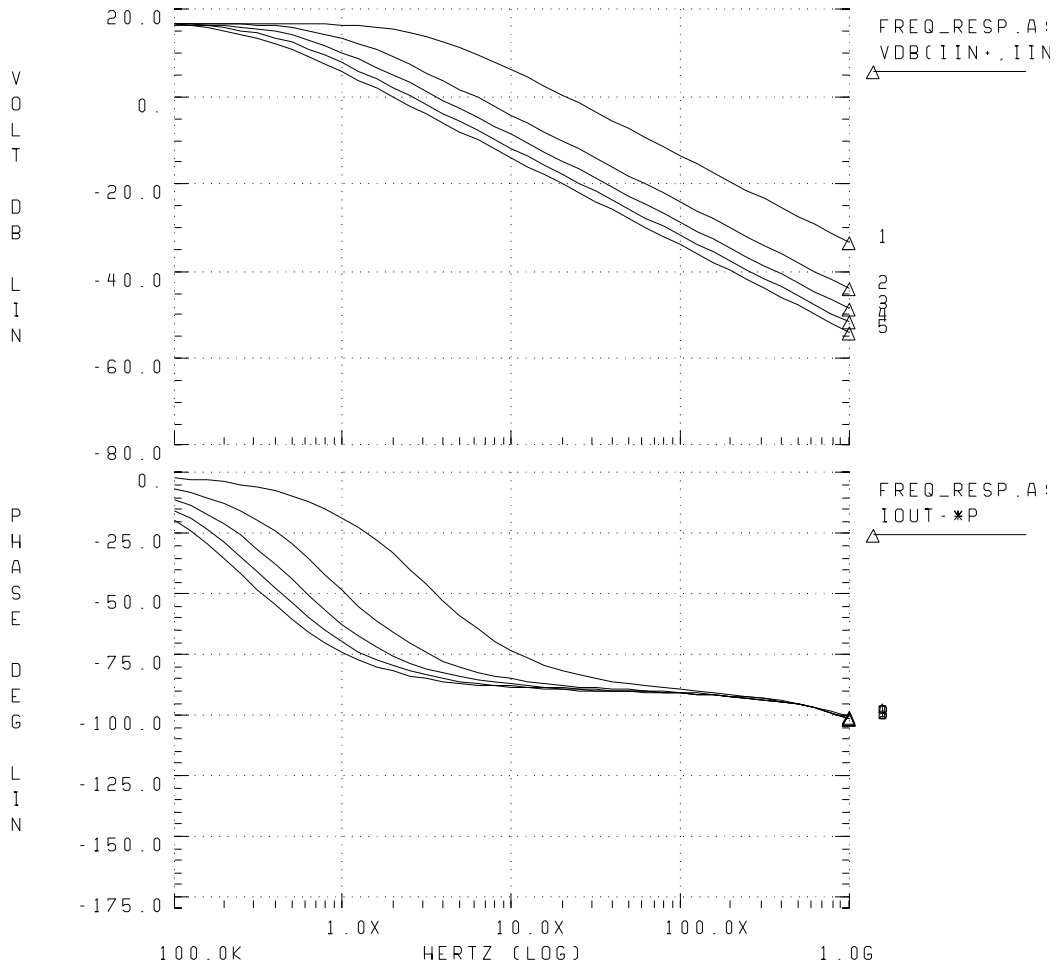

Fig. 6.13 – Frequency response of the area integrator
for nominal integrating capacitance values.

Transient response

The plot in Fig. 6.14 shows the transient response of the integrator to a five cycle long burst for the same capacitance values. A 10 MHz rectified pulse sequence consisting of measured data obtained from an actual read head has been used to simulate the input servo burst. The optimum compromise between the minimum number of used pulses and the output precision depends on the channel frequency and can ultimately be tuned by the DSP through feedback control of the capacitor array.

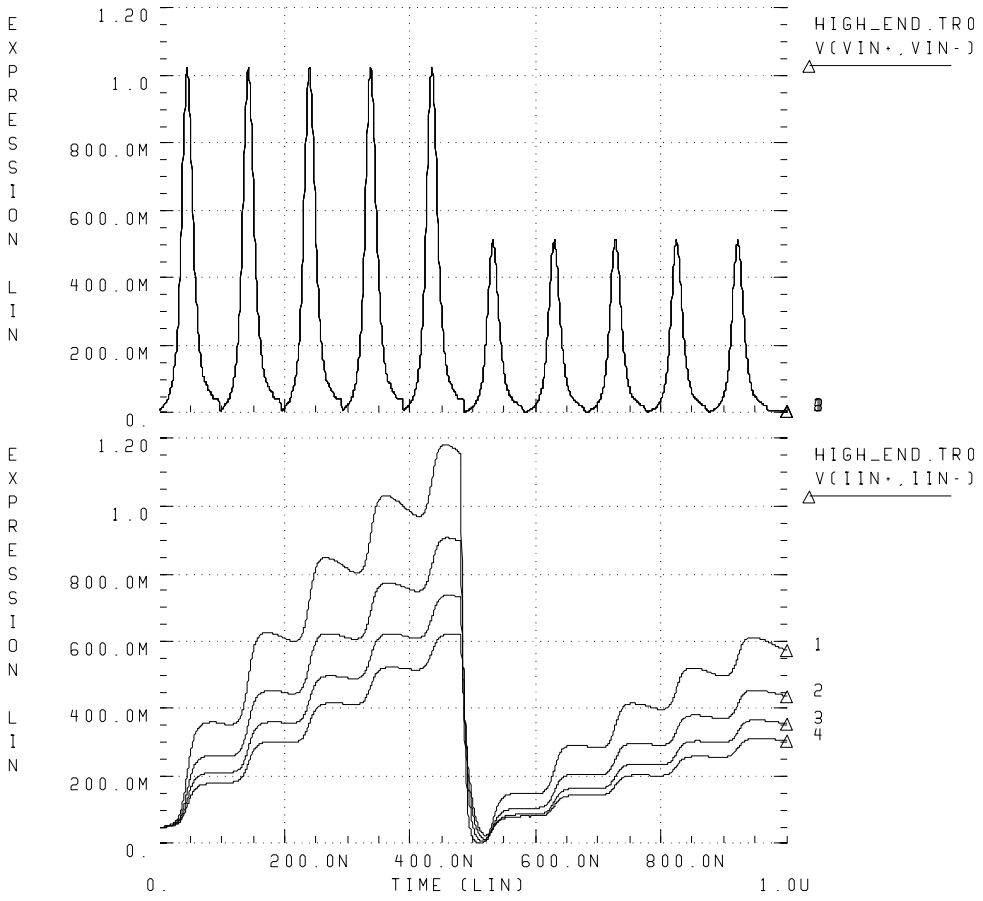

Fig. 6.14 – Transient response of the area integrator to a sequence of Lorentzian pulses for integrating capacitance values of 10pF, 20pF, 30pF, 40pF.

Table 6.1 resumes the main electrical characteristics of the area integrator cell including CMRR, PSRR, GSRR, THD and power dissipation.

Table 6.1 – Main characteristics of the area integrator filter.

Technology	0.5 μm Digital MOS
Pole Frequency	1 to 400 MHz
CMRR	80 dB
PSRR, GSRR	60 dB
THD	– 50 dB
Power supply	3.0 V
Power dissipation	3.0 mW
Tuning Bits	8
Active area	0.2x0.3 mm^2

Several read channels with integrated servo demodulation provide these special signals separately, being the most common configurations, either parallel and asynchronous bursts, single ended or differential signals.

This continuous-time solution for servo burst demodulation using area detection averages the contribution of several pulses thus reducing random noise sensibility and eliminating the dependence of the sampled voltage on the shape of the last pulse. This scheme can easily be processed asynchronously requiring only a small number of cycles for each servo burst. The circuit features a flexible low-power and small size die, and can easily be embedded in a read channel with integrated servo controller.

*6.3 Experimental results of MDFE equalizer (***MDFE–04***)*

The goal of this integrated circuit was to conceive, design and test a low voltage low power adaptive continuous-time third order allpass equalizer implemented in a 0.5μm standard digital CMOS technology.

Two similar IC's have been designed and passed on to fabrication:

- ***MDFE–AP02*** is a 3.88x4.47 mm^2 die designed in ECAD06 technology, a 0.6µm standard digital CMOS process with one polysilicon layer and two metal layers. This circuit was designed for production in ATMEL/Rousset facilities.
- ***MDFE–AP04*** is a 2.24x2.24 mm^2 square die realized in ECAT05 technology, a 0.5µm standard digital CMOS process with two polysilicon layers and three metal layers, and has been fabricated in ATMEL/Colorado facilities.

Both circuits include the same test structures and auxiliary circuits, and differ mainly in layout rules, die size and package. The printed circuit board (PCB) sketched for the probing of these IC's is shown in figures Fig. 6.17 and Fig. 6.16.

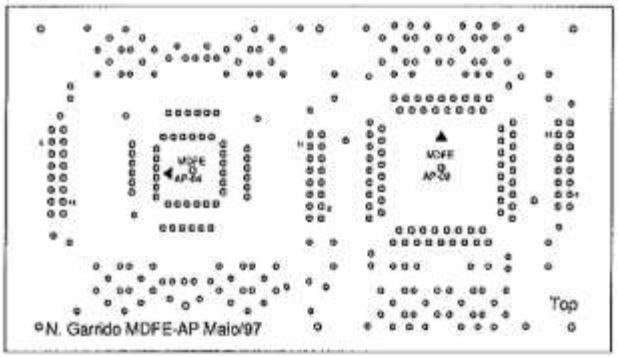

Fig. 6.15 – PCB layout top view.

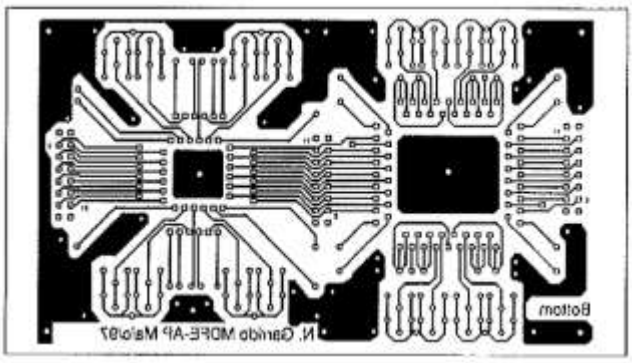

Fig. 6.16 – PCB layout bottom view.

Although MDFE-AP02 was totally designed, the ECDM05 and ECAD06 processes at Roussets facilities were discontinued when ATMEL bought the factory, hence the chip

was redesigned for process ECAT05 and later fabricated in Colorado Springs factory under the name MDFE-AP04. Both designs include four basic test blocks as can be seen in the layout floor plan depicted in Fig. 6.17.

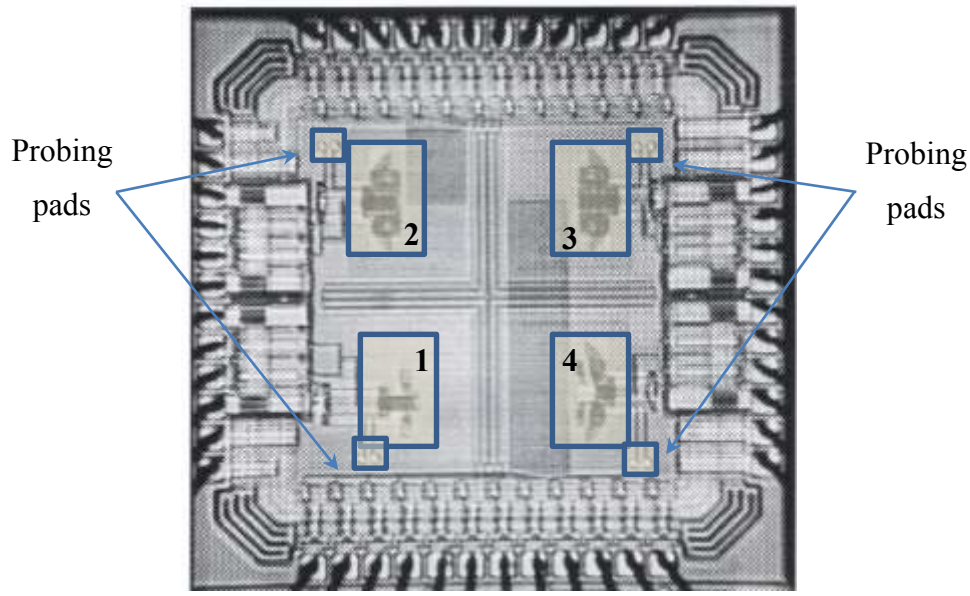

Fig. 6.17 – Layout and floor-plan of MDFE-04.

- ***Block 1*** – ***A non-programmable orthonormal equalizer*** used to debug the system in the case of a non-predicted error in the adaptation circuitry.
- ***Block 2*** – ***An orthonormal structure allpass equalizer*** for use in a MDFE magnetic disk read channel.
- ***Block 3*** – ***A canonic structure allpass equalizer*** for recursive filter structure comparison and debugging.
- ***Block 4*** – ***A transconductor cell*** to test the behavior and frequency limitations of this architecture. This block also realizes a one pole and can be used as a variable gain integrator for servo burst demodulation.

MDFE–AP02 integrated circuit

The MDFE–AP02 circuit was originally designed for ES2/ECDM05 process and was resimulated and layout level adjusted to concur with ATMEL/ECDM06 models. Since ECDM05 technology was prematurely discontinued and the surrogate process ECAD06 had poor market acceptance, the MDFE–AP02 IC was stranded in Rousset's production line for several months and was never fabricated, and therefore no engineering samples where produced for test purposes. The advent of ATMEL/ECAT05 technology apparently made the debuting ECAD06 process obsolete at naissance and hence the MDFE–AP04 integrated circuit was designed to accelerate testing. As a result, no experimental measurements of MDFE–AP02 performance have been executed to compare with the simulation results. The testing conditions and equipment setup are coincident with those further described for MDFE-AP04 and thus the test board was made to fit both circuits with the expectation that test samples for both circuits would eventually be available.

MDFE–AP04 integrated circuit

The MDFE–AP04 IC is a ported version of MDFE–AP02 to ATMEL/ECAT05 process. This circuit comprises the same four basic blocs as the previous design, likewise geometrically disposed as they are represented in Fig. 6.18.

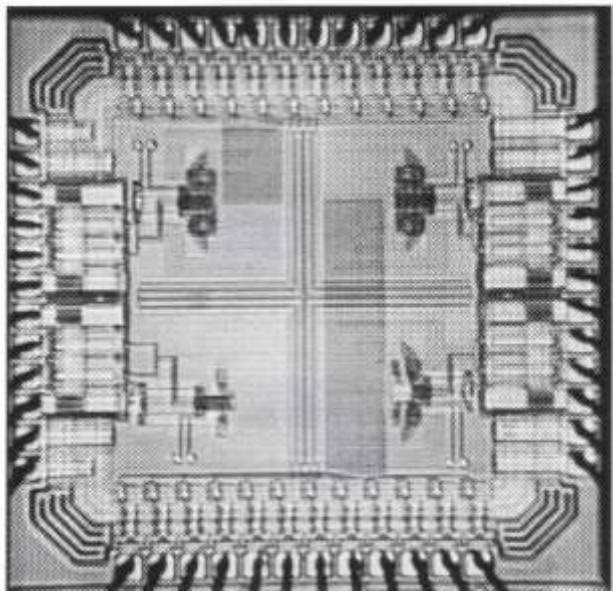

Fig. 6.18 – Top view of MDFE-04.

The simulation result for the balanced output of the orthonormal structure studied in 5.7 for the MDFE equalizer is depicted in Fig. 6.19. A similar behavior was observed in the measured result.

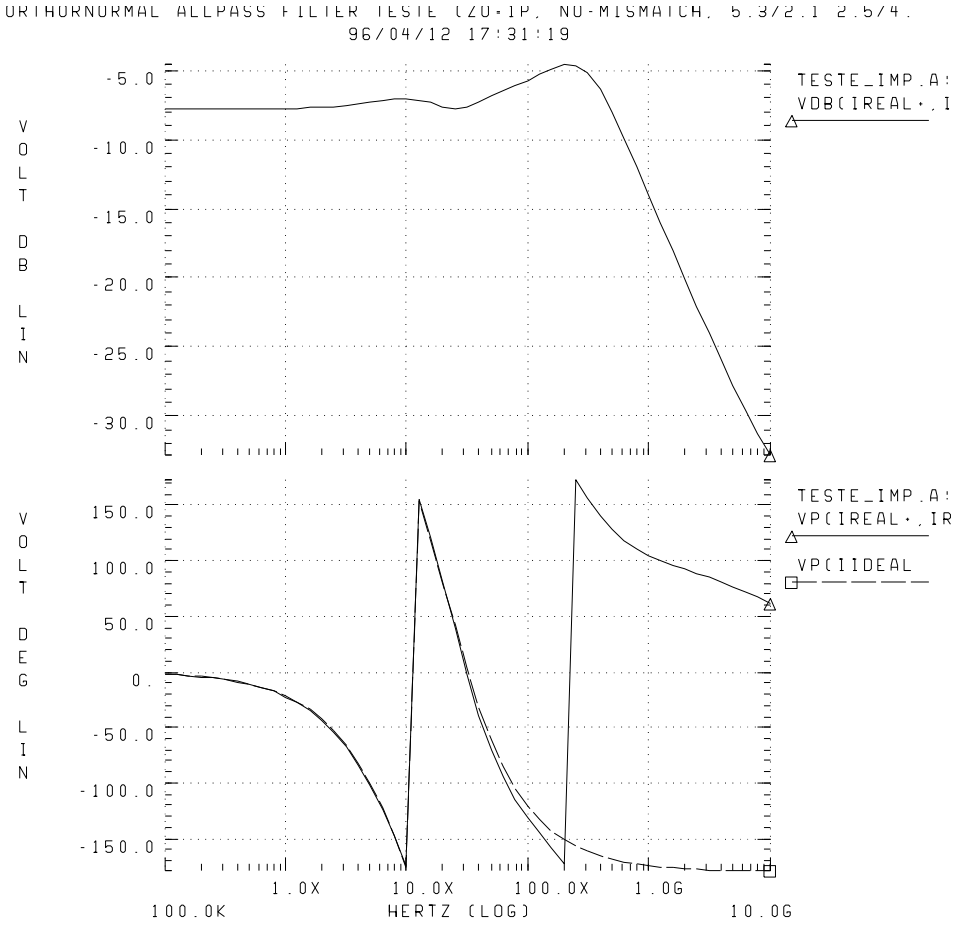

Fig. 6.19 – Simulated frequency response of the allpass filter (I_{real} and I_{ideal}).

Self-biased trasconductor for VHF applications

To implement these equalizers the fundamental block is the transconductor cell. For this project, a transconductor was designed capable of very high frequency operation for low voltage, low power behavior in standard 0.5μm CMOS digital technology. The basic circuit was presented in [6.8] and described in section 4.6. The main electrical characteristics of the transconductor are difficult to observe, for this project we included an additional open-output transconductor cell available throw micro pads inside the die, only available for test with pico-probe testing. The test setup is shown in figures Fig. 6.20 and Fig. 6.21.

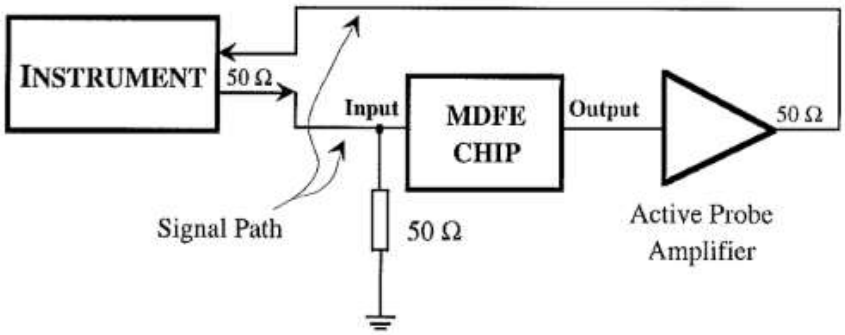

Fig. 6.20 – Setup for MDFE pico-probe setup.

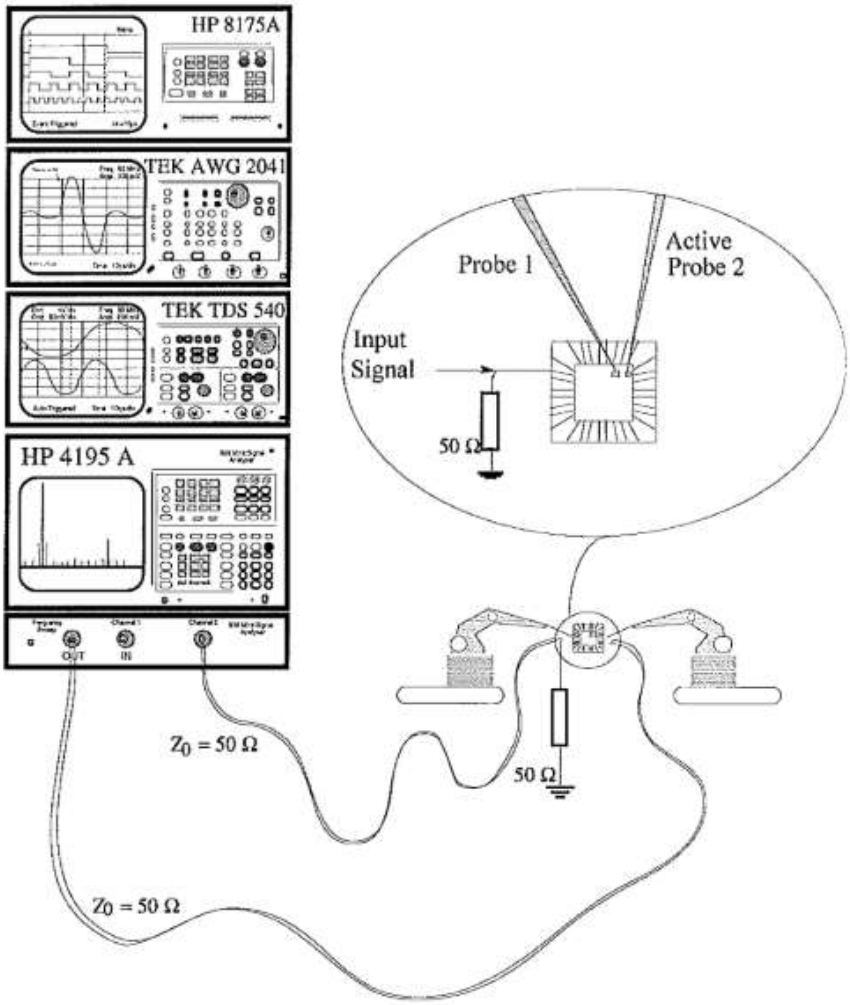

Fig. 6.21 – MDFE-04 test setup.

The expected DC sweep analysis of the device for the negative and positive voltage outputs (considering open circuit load at the current outputs) is depicted in Fig. 6.22. The voltage input are used to identify the 1.4V biasing input voltage for the feedback loops of the self-biased device.

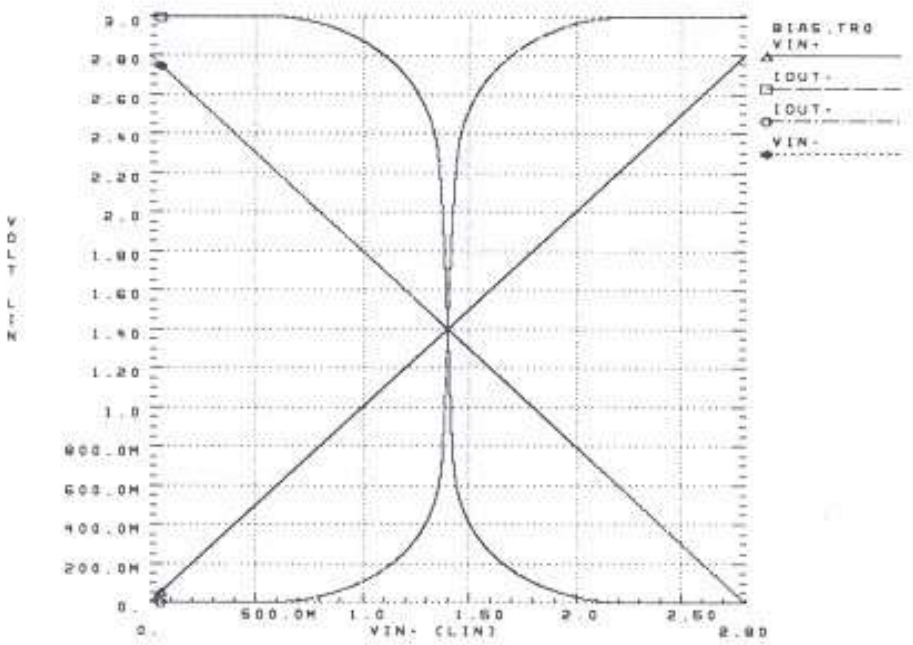

Fig. 6.22 – Simulation result for the DC characteristic of the transconductor cell.

Fig. 6.23 shows the experimental measurements on I_{out+} and I_{out-} for an input differential voltage swing 1Vpp, using 1.4V as analog ground (0V on the diagram). The output has a 1:10 attenuation factor due to the oscilloscope probe gain, hence, the results closely match the simulation data. The measured low frequency differential output voltage gain for the open output transconductor is approximately 30dB, confirming the values in figures Fig. 6.22 and Fig. 6.24.

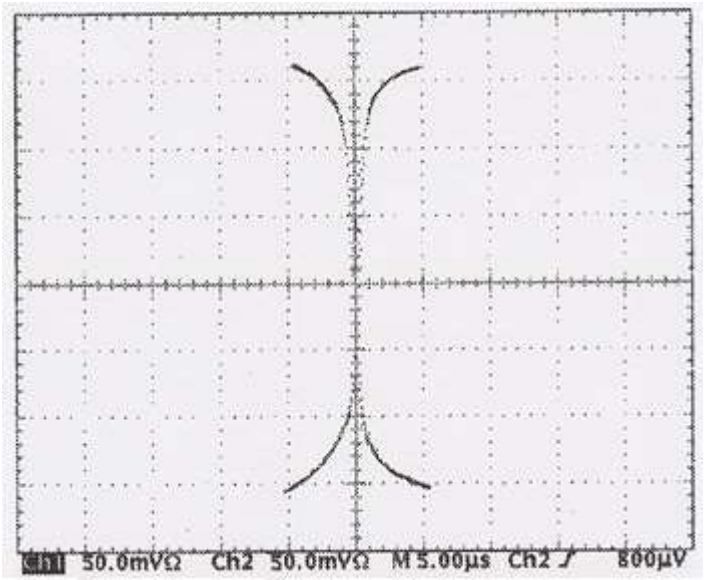

Fig. 6.23 – Measured result of the DC characteristic of the transconductor cell.

Fig. 6.24 shows the simulation results for the open output transcondutor cell considering ideal measuring capability. Considering the measured system with a pico-probe, we should assume approximately 0.5pF for the parasitic value of the pico-probe.

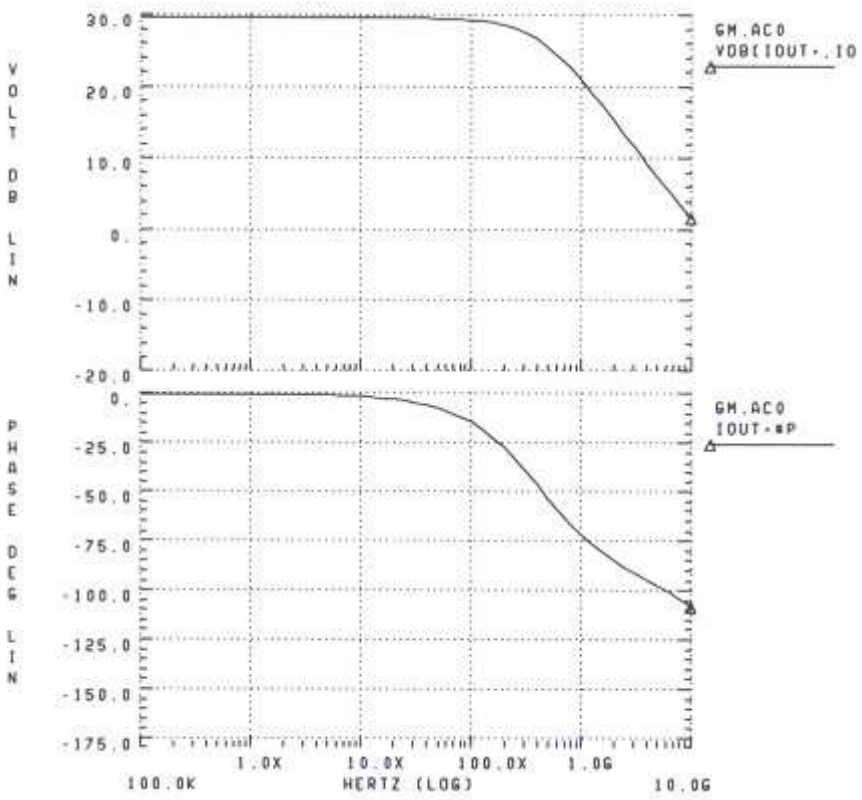

Fig. 6.24 – Frequency response of the pseudo-differential transconductor.

The simulated value for both balanced outputs was simulated considering this value (0.5pF) for the pico-probe. The positive and negative output of the transconductor show a pole at approximately 1MHz, and nearly perfect behavior until 100MHz as shown in Fig. 6.25.

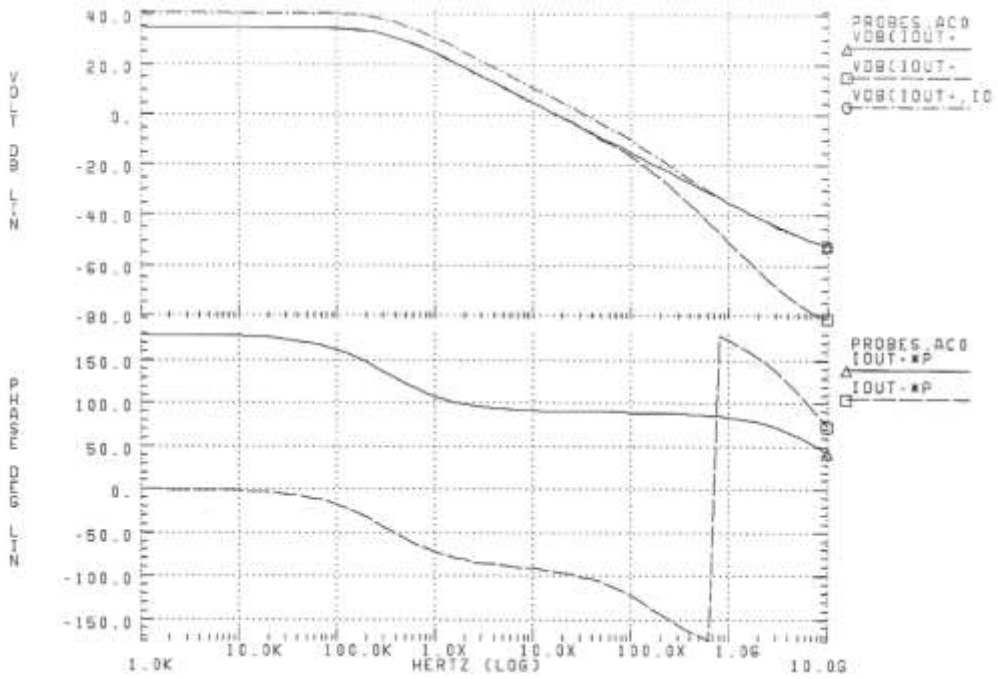

Fig. 6.25 – Simulation results for the frequency response of the transconductor cell (I_{out+} and I_{out-}).

The same behavior was also observed in the measured pico-probe data for the negative and positive outputs as seen in figures Fig. 6.26 and Fig. 6.27. The values are good until approximately 80MHz where an electromagnetic coupling is sensed at the output due to the testing procedure.

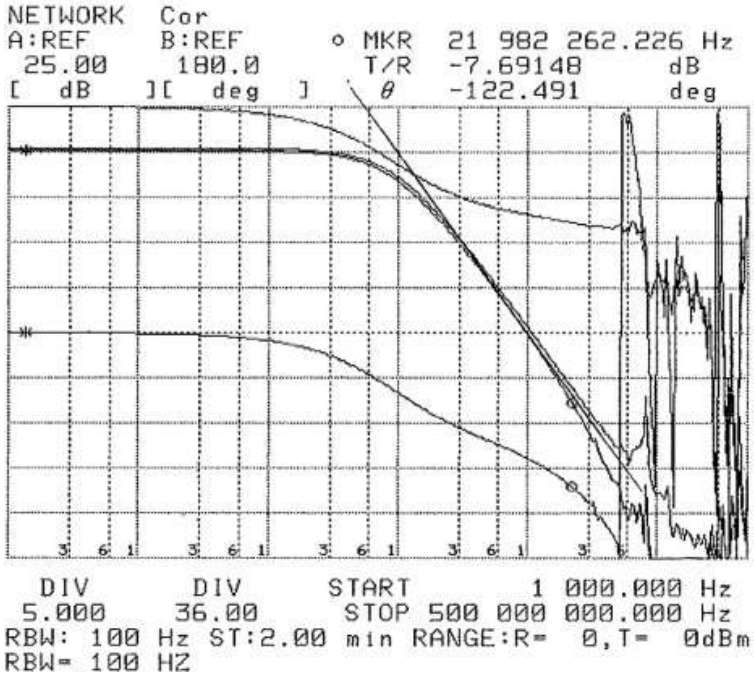

Fig. 6.26 – Frequency response of the transconductor cell (I_{out+} and I_{out-}).

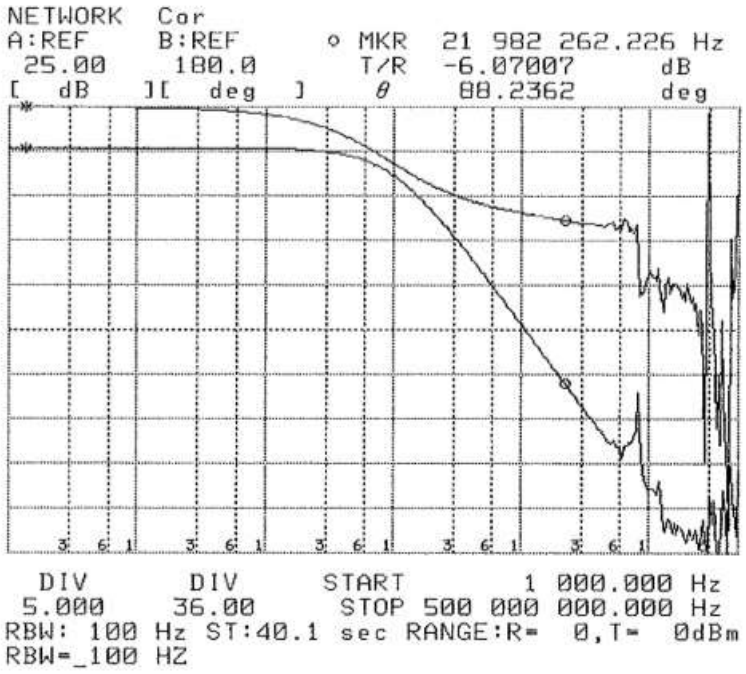

Fig. 6.27 – Frequency response of the transconductor cell (I_{out+}).

The deformation on the response observed at approximately 81MHz is due to the test procedure. Electromagnetic coupling from the pico-probe to the bonding wire is responsible for both the peak in the amplitude and the phase shift observed in figures Fig. 6.26 and Fig. 6.27.

The coupling was tested by disconnecting the probe from the pad but keeping it close to the bonding pad and bonding wires.

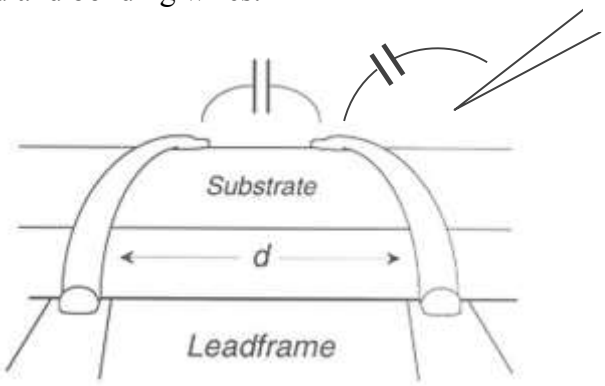

Fig. 6.28 – Bonding wire and pico-probe electromagnetic coupling.

Fig. 6.29 shows the radiated power received on the output. The output voltage showed non-neglectable coupling at 81MHz thus explaining the observed effect on the output.

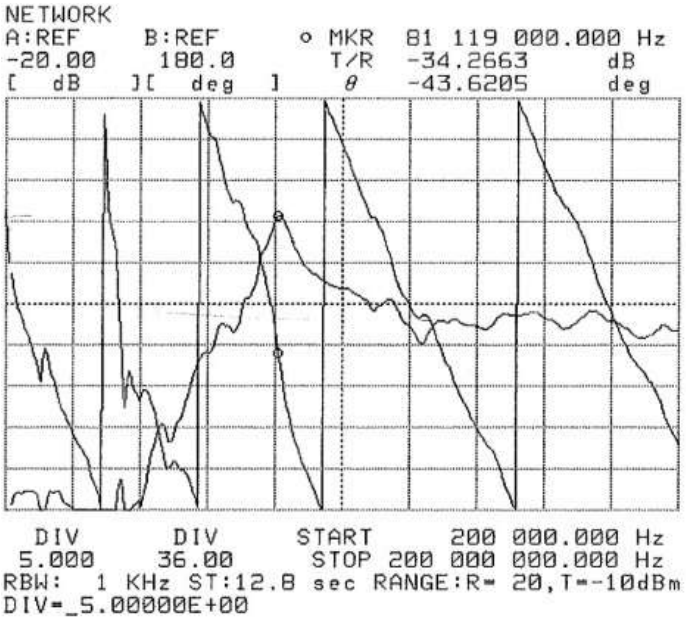

Fig. 6.29 – Coupling effect of pico-probe at 80MHz.

This effect is caused by the test procedure, hence, it would not affect the expected results of the transconductance cell.

Harmonic distortion was tested on the input at 1Vpp@1MHz. The output shows negligible second order harmonic distortion and reduced third order harmonic distortion, for an overall total harmonic distortion base line under -52dB.

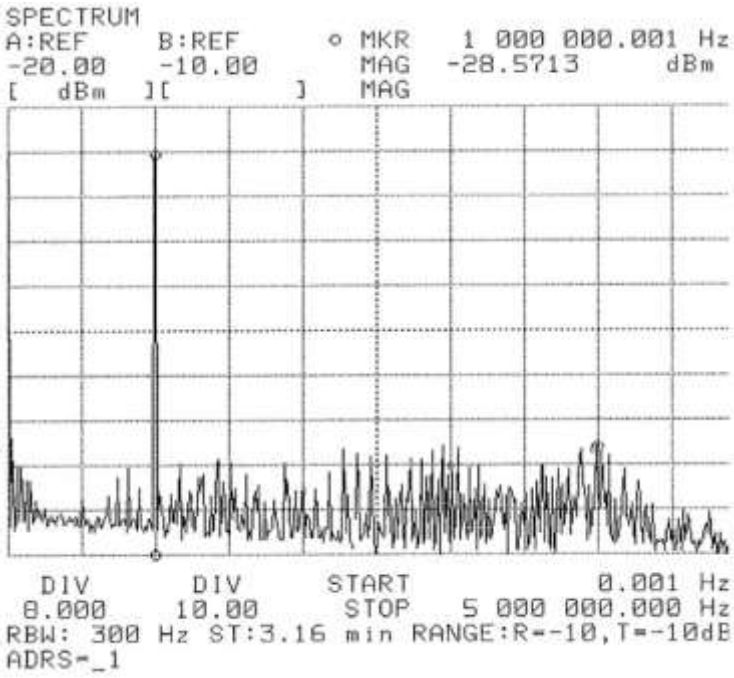

Fig. 6.30 – Harmonic distortion of the transconductor cell.

The basic electrical characteristics including PSRR, GSRR, THD and power dissipation of the transconductor are summarized in Table 6.2.

Table 6.2 – Electrical characteristics of the transconductor cell.

Technology	0.5μm Digital CMOS
Supply Voltage	3.0 V
PSRR, GSRR	50 dB
THD (1Vpp@1MHz)	–52 dB
Power dissipation	350 μW

6.4 Master-Slave topology filter combined with a bandgap voltage reference

Finally, we tested a tuned filter strategy based on a bandgap voltage reference and on a *Master-Slave* filter. This technique was implemented with success on an active OPAMP-RC filter designed txumtspci designed in 2000 at Chipidea using ATMEL/at57500 process for an UMTS transmit channel capable of tuning the filter time constant. A bandgap voltage reference was designed and tested using ATMEL/ECAT05 process. The basic design options and experimental data are available in annex B.

6.5 Conclusions

In this thesis we presented two fully analog continuous-time integrated adaptive filters for the implementation of an allpass forward equalizer for MDFE in hard disk drive read-channels. Both current mode state-space recursive filters where simulated at transistor level showing equivalent equalization response to partial response systems, whilst reducing consumption by a factor of 10 to 100 compared to conventional FIR digital equalizers. LMS modified algorithms allowing the automatic tuning of the poles frequency can compensate process tolerances that influence the effective value of the active devices and capacitors. Both equalizers are implemented using current mode continuous-time *gm*-C filters operating at very high frequency combined with biased MOSFET capacitor arrays in standard digital CMOS technology with low supply voltage. The goal of this work was

to conceive, design and test a low voltage low power adaptive continuous-time third order allpass equalizer implemented in a 0.5μm standard digital CMOS technology.

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Chapter 7

Conclusions and future work

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7.1 Conclusions

The overall development goal in disk drive technology is to reduce device size and power consumption and to increase data rates and storage capacity. An exponential evolution has characterized the market offers in each of these requirements. Portable computers are the growing and profitable market off the coming years, and accordingly *Low end* drives come out as the most interesting area of study.

The strive towards denser storage and higher data-transfer rates coincides with the decline of conventional peak-detection acquisition front-ends, giving way to improved reliability data schemes. Various data recovery schemes based on Decision Feedback Equalization (DFE) and Partial Response Maximum Likelihood (PRML) have been presented.

These schemes compensate the expected Intersymbol Interference (ISI) between input-pulses, akin to high-speed acquisition. The drawbacks of these architectures, such as high silicon area (and thus high cost) and high power consumption on high frequency channels, have been studied and combated in this work through the use of analog CMOS circuitry.

The projected circuits MDFE–AP02 and MDFE–AP04, have been designed to be used as the forward equalizer block in a MDFE based read channel. These equalizers contain low-voltage low-power adaptive continuous-time third order allpass equalizers capable of achieving the desired equalized output response target in [7.1].

A 2^{nd} order and two 3^{rd} recursive current-mode filters were designed and simulated [7.2][7.3]. All designs feature very high frequency, low power consumption and low supply voltage using adaptive state-space recursive filters based on current-mode *gm*-C structures.

For the third order systems a canonical (companion) solution and an orthonormal solution where designed and simulated. Besides its improved adaptability, the orthonormal structure shows improved frequency response over the canonical structure and hence suggests that the orthonormal structure is a better realization of the allpass forward equalizer, especially at higher data rates as shown in [7.2].

The continuous time approach developed in this thesis can reduce consumption by a factor of 10 compared to FIR equivalent filtering. The equalizer can work at very high frequencies at low supply voltages (as low as 1.8V). The filter can be used on a MDFE read channel [7.2][7.3].

Keeping in mind that power consumption of the active elements is, in the long term, the key factor for the final acceptance of the proposed solution, further confirms the reasonability of using digital CMOS technology has shown in[7.4], capable of implementing the continuous-time current-mode MDFE equalizers. The transconductor cell is a low power, low voltage, fully balanced cell working at very high frequency for high bandwidth behavior *gm*-C filters.

The auto-biasing is granted by feedback loops, thus avoiding common-mode circuitry and yielding improved stability and noise immunity. The proposed transconductor can operate at low supply voltages for reduced power dissipation. The small feature transistors are designed to allow good high frequency operation while controlling mismatch effects. Computer simulations show [7.4][7.5][7.6] that this transconductor is capable of sustaining correct operation for supply voltages as low as 1.8V.

An application example for the implementation of an area integrator servo burst demodulator for hard disk drives has been presented in [7.5][7.7][7.8] using the proposed transconductor cell. This solution uses a continuous time first order *gm*-c filter to implement a one-pole integrator block capable of performing the area integration function.

7.2 Future research suggestions

Low end drives aim especially at low power operation and small size devices (preferentially using single disk drives), at the cost of low storage capacity. *High end and Medium performance* drives are also reducing power and size, but at lower rate focusing mainly on huge capacity devices and fast data transfer rates.

The predictable future for Low-Performance drives is that a low power single mixed signal CMOS integrated circuit will include all the referred electronic blocks (except for the spindle and head drivers) and substitute the actual 7 to 12 chip solutions with simpler and cheaper 2 or 3 chip implementations.

The drawing of research scenarios and the pointing out of the most significant spots within science's study path is a critical requirement for the grasp of revitalized brain-power, and ultimately the essence of development. Therefore, the author wishes to propose a more comprehensive cogitation on the following subjects, whereas he feels that the urgency of such matters has become apparent.

Silicon implementation of a fully integrated mixed-signal disk-drive manager CHIP

Including all digital and analog functionality (e.g. read/write channel, servo demodulator, host interface DSP, memory) this complete design solution has been anxiously yearned for by hard disk manufacturing companies, and represents a considerable challenge since it requires extremely small device size technology (under 0.35 μm) considering the inherent complexity of the digital system, and especially due to very low supply voltage (probably under 1.8V) operation in a high frequency mixed signal IC.

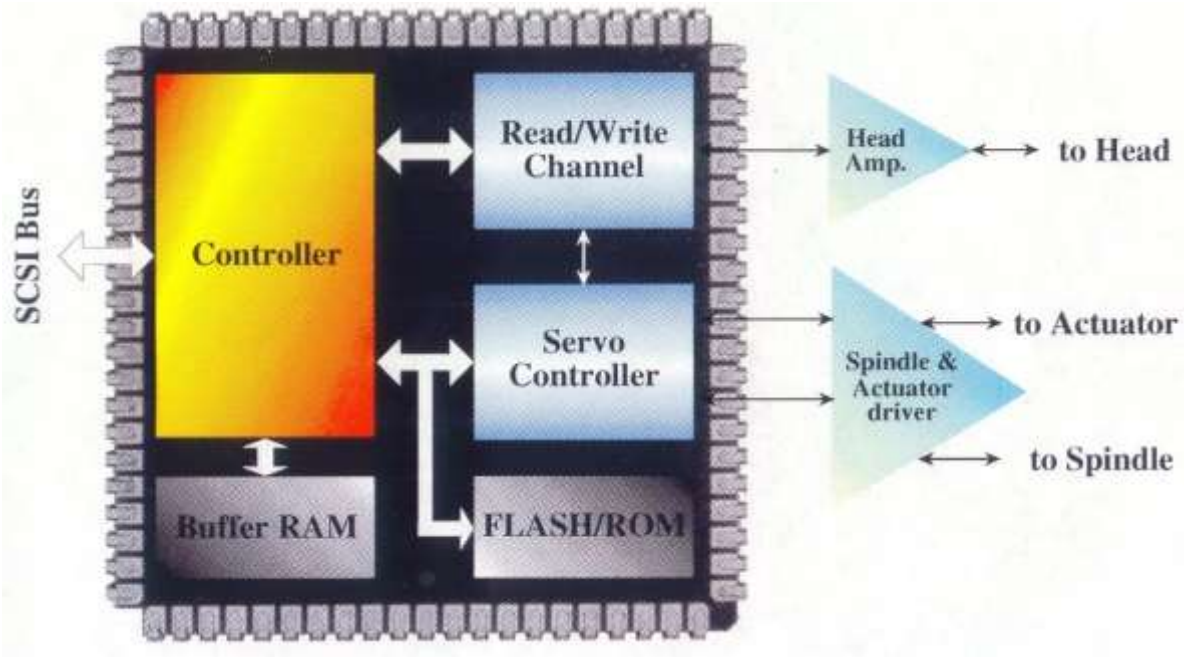

Fig. 7.1 – Disk-drive electronic blocks diagram.

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Annex A: Differential pair

Differential pair in bipolar technology

The emitter-coupled differential pair transconductor Fig. A.1 is the basis from where all other more complex structures have evolved. It is a very simple and well known device consisting of a biasing current source I and two emitter-coupled NPN transistors. We will derive the expressions for NPN differential pair, that would be analogous for a vertically symmetrical circuit using a PNP differential pair.

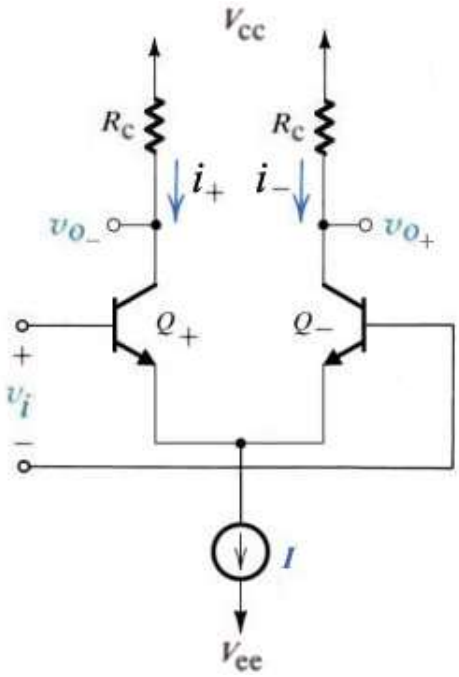

Fig A.1 – Schematic of a differential pair in bipolar technology.

The differential input voltage of the differential pair can be defined as

$$v_i = v_{BE_+} - v_{BE_-}. \tag{7.1}$$

and the collector currents of the differential pair are given by

$$i_{C+} = I_S \cdot \ell^{\frac{v_{BE+}}{V_T}} \tag{7.2}$$

$$i_{C-} = I_S \cdot \ell^{\frac{v_{BE-}}{V_T}} . \tag{7.3}$$

The saturation current I_S and the thermal voltage V_T in these equations are given by equations (7.4) and (7.5):

$$I_S = \frac{A_E \cdot q \cdot D_n \cdot n_i^{\,2}}{N_A \cdot W} \tag{7.4}$$

where A_E emitter area, [m^2]

q electron charge, [C]

D_n electron diffusivity, [m^2/s]

n_i intrinsic concentration, [1/m^3]

N_A acceptor concentration, [1/m^3]

W effective base width, [m]

$$V_T = \frac{k \cdot T}{q} \tag{7.5}$$

where k Boltzmann's constant, [J/C]

T temperature, [K]

q electron charge, [C]

Continuity at the common emitter node imposes that

$$I = i_{E_+} + i_{E_-} \tag{7.6}$$

Assuming that the transistors of the differential pair are working in the forward region

$$i_C = \alpha_F \cdot i_E \tag{7.7}$$

Combining equations (7.6) and (7.7)

$$I = \frac{i_{C_+}}{\alpha_F} + \frac{i_{C_-}}{\alpha_F} = \frac{i_{C_+}}{\alpha_F} + \frac{I_S}{\alpha_F}\,\ell^{\frac{v_{BE-}}{V_T}} \tag{7.8}$$

$$I = \frac{i_{C_+}}{\alpha_F} + \frac{I_S}{\alpha_F}\,\ell^{\frac{v_{BE+}-v_i}{V_T}} \tag{7.9}$$

and hence

$$\alpha_F \cdot I = i_{C_+} + i_{C_+} \cdot \ell^{-\frac{v_i}{V_T}} \tag{7.10}$$

$$\alpha_F \cdot I = i_{C_+}\left(1 + \ell^{-\frac{v_i}{V_T}}\right) \tag{7.11}$$

the collector currents i_{C_+} and i_{C_-} are given by:

$$i_{C_+} = \frac{I \cdot \alpha_F}{\left(1 + \ell^{-\frac{v_i}{V_T}}\right)} \tag{7.12}$$

$$i_{C_-} = \frac{I \cdot \alpha_F}{\left(1 + \ell^{\frac{v_i}{V_T}}\right)} \tag{7.13}$$

The differential output current of the common emitter pair defined as $i_O = i_{C+} - i_{C_-}$ can be derived from (7.12) and (7.13)

$$i_O = \left(\frac{I \cdot \alpha_F}{\left(1 + \ell^{-\frac{v_i}{V_T}}\right)} - \frac{I \cdot \alpha_F}{\left(1 + \ell^{\frac{v_i}{V_T}}\right)}\right) \tag{7.14}$$

$$i_O = I \cdot \alpha_F \cdot \frac{\left(1+\ell^{\frac{v_i}{v_T}}\right)-\left(1+\ell^{-\frac{v_i}{v_T}}\right)}{\left(1+\ell^{\frac{v_i}{v_T}}\right)\cdot\left(1+\ell^{-\frac{v_i}{v_T}}\right)} \tag{7.15}$$

Simplifying this equation we obtain

$$i_O = \alpha_F \cdot I \cdot \frac{\ell^{\frac{v_i}{v_T}}-\ell^{-\frac{v_i}{v_T}}}{\ell^{\frac{v_i}{v_T}}+2+\ell^{-\frac{v_i}{v_T}}} \tag{7.16}$$

$$i_O = \alpha_F \cdot I \cdot \frac{\left(\ell^{\frac{v_i}{2v_T}}+\ell^{-\frac{v_i}{2v_T}}\right)\cdot\left(\ell^{\frac{v_i}{2v_T}}-\ell^{-\frac{v_i}{2v_T}}\right)}{\left(\ell^{\frac{v_i}{2v_T}}+\ell^{-\frac{v_i}{2v_T}}\right)^2}. \tag{7.17}$$

Using the definition of hyperbolic tangent, given by $\tanh(x)=\frac{\ell^x-\ell^{-x}}{\ell^x+\ell^{-x}}$ this equation can be more easily represented as

$$i_O = \alpha_F \cdot I \cdot \frac{\ell^{\frac{v_i}{2v_T}}-\ell^{-\frac{v_i}{2v_T}}}{\ell^{\frac{v_i}{2v_T}}+\ell^{-\frac{v_i}{2v_T}}} = \alpha_F \cdot I \cdot \tanh\left(\frac{v_i}{2v_T}\right). \tag{7.18}$$

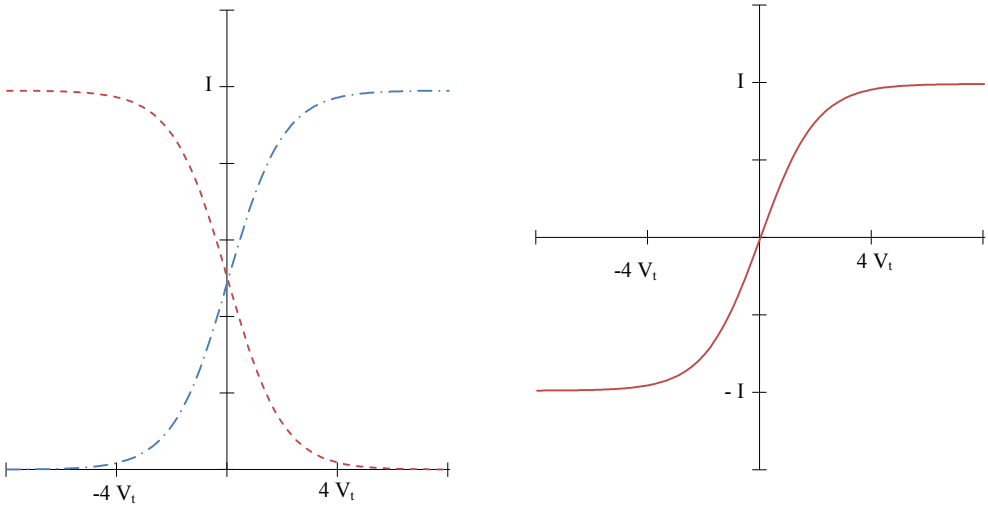

Fig. A.2 – Current output of an ideal differential-pair transconductor.

Differential pair in CMOS technology

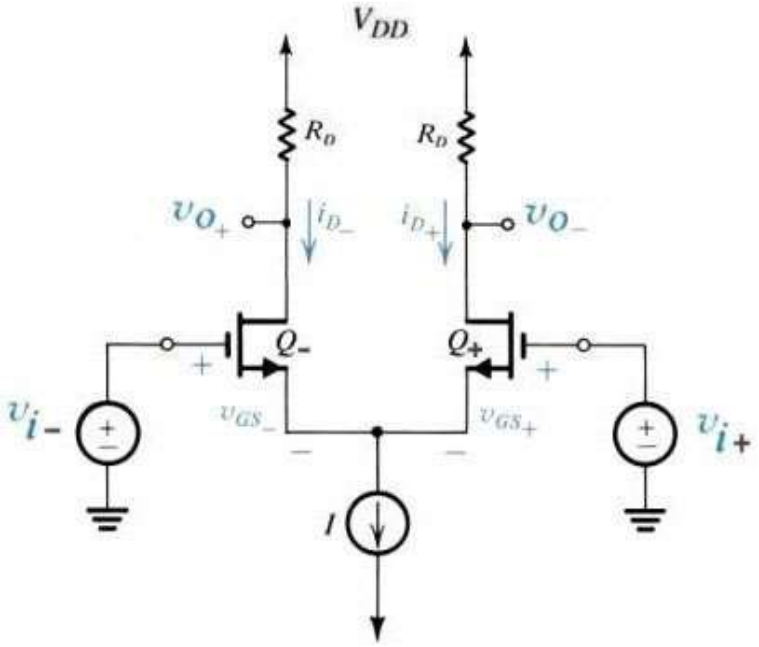

Fig. A.3 – Schematic of a differential pair in CMOS technology.

The ideal transfer characteristic of the MOS differential pair can be derived in a similar manner as shown for its bipolar realization. Assuming that the source coupled

MOS transistors are working in the saturation region and defining the drain currents of the source coupled MOS transistors i_+ and i_- yields:

$$i_{d_+} = k \cdot \left(v_{gs_+} - V_t\right)^2 \qquad \text{and} \qquad i_{d_-} = k \cdot \left(v_{gs_-} - V_t\right)^2 \tag{7.19}$$

where $k = \frac{k_n}{2} \cdot \frac{W}{L}$ for both transistors assuming equal dimensions.

Continuity at the source node of the differential pair imposes that

$$I = i_{d_+} + i_{d_-} . \tag{7.20}$$

The input voltages v_{i_+} and v_{i_-} at the gates of the differential pair must have a common DC biasing voltage as given by

$$v_{i_+} = v_{gs_+} + V_S \qquad \text{and} \qquad v_{i_-} = v_{gs_-} + V_S . \tag{7.21}$$

The differential input voltage can be defined as

$$v_i = v_{i_+} - v_{i_-} \qquad \Rightarrow \qquad v_i = v_{gs_+} - v_{gs_-} . \tag{7.22}$$

Combining equations (7.19)-(7.20) with (7.22) yields

$$I = i_{d_+} + k \cdot \left(v_{gs_-} - V_t\right)^2 \qquad \Rightarrow \qquad I = i_{d_+} + k \cdot \left(v_{gs_+} - v_i - V_t\right)^2 \tag{7.23}$$

which can be simplified using (7.19)

$$I = 2 \cdot i_{d_+} - 2k \cdot \left(v_{gs_+} - V_t\right) \cdot v_i + k \cdot v_i^{\,2} \quad \Rightarrow \quad 0 = i_{d_+} - v_i \cdot \sqrt{k} \cdot \sqrt{i_{d_+}} + \frac{k \cdot v_i^{\,2} - I}{2} \tag{7.24}$$

Solving (7.24) in respect to $\sqrt{i_{d+}}$ we can derive the i_{d+}value of i_{d+}

$$\sqrt{i_{d_+}} = \frac{v_i}{2}\sqrt{k} \pm \sqrt{\frac{k \cdot v_i^{\,2}}{4} - \frac{k \cdot v_i^{\,2} - I}{2}} \qquad \Rightarrow \quad \sqrt{i_{d_+}} = \frac{v_i}{2}\sqrt{k} \pm \sqrt{\frac{I}{2} - \frac{k \cdot v_i^{\,2}}{4}} \tag{7.25}$$

$$i_{d_+} = \frac{v_i^{\,2}}{4}k + \frac{I}{2} - \frac{k \cdot v_i^{\,2}}{4} \pm v_i \cdot \sqrt{k} \cdot \sqrt{\frac{I}{2} - \frac{k \cdot v_i^{\,2}}{4}} \quad \Rightarrow \quad i_{d_+} = \frac{I}{2} \pm v_i \cdot \sqrt{k} \cdot \sqrt{\frac{I}{2} - \frac{k \cdot v_i^{\,2}}{4}} \tag{7.26}$$

only the positive solution is valid, hence

$$i_{d_+} = \frac{I}{2} + v_i \cdot \sqrt{k} \cdot \sqrt{\frac{I}{2} - \frac{k \cdot v_i^{\,2}}{4}} \,. \tag{7.27}$$

analogously i_{d-} is given by

$$i_{d_-} = \frac{I}{2} - v_i \cdot \sqrt{k} \cdot \sqrt{\frac{I}{2} - \frac{k \cdot v_i^{\,2}}{4}} \tag{7.28}$$

The differential output current of the differential pair i_o is defined as

$$i_o = i_{d_+} - i_{d_-} \tag{7.29}$$

yielding

$$i_o = 2 \cdot v_i \cdot \sqrt{k} \cdot \sqrt{\frac{I}{2} - \frac{k \cdot v_i^{\,2}}{4}} \tag{7.30}$$

or simply

$$i_O = v_i \cdot \sqrt{2k \cdot I - k^2 \cdot v_i^{\,2}} \,. \tag{7.31}$$

The values of v_i that lead to total disequilibria of the differential pair impose that $i_{d_-} = 0$ or $i_{d_-} = I$. Using equation (7.28) we can easily derive that

$$\frac{I^2}{4 \cdot v_i^{\,2} \cdot k} = \frac{I}{2} - \frac{k \cdot v_i^{\,2}}{4} \qquad \Rightarrow \qquad 0 = I^2 - 2 \cdot I \cdot v_i^{\,2} \cdot k + v_i^{\,4} \cdot k^2 \tag{7.32}$$

$$0 = \left(I - v_i^{\,2} \cdot k\right)^2 \qquad \Rightarrow \qquad v_i = \pm\sqrt{\frac{I}{k}} \,. \tag{7.33}$$

These values define the dominium of applicability of equations (7.27)-(7.32) and correspond to the boundary operating conditions of the differential pair.

The value of v_i may be given as a function of V_{GS} or $V_{GS_{Total}}$, corresponding to the equilibrium state of the differential pair for $i_{d_+} = i_{d_-} = \frac{I}{2}$ and $v_{gs_+} = v_{gs_-} = V_{GS}$, or corresponding to the total unbalance input, $I = i_{d_+} = k \cdot \left(V_{GS_{Total}} - V_t\right)^2$, thus we can derive:

$$v_i = \pm\sqrt{\frac{2 \cdot k \cdot \left(V_{GS} - V_t\right)^2}{k}} = \pm\sqrt{2} \cdot \left(V_{GS} - V_t\right) \tag{7.34}$$

$$v_i = \pm\sqrt{\frac{k \cdot \left(V_{GS_{Total}} - V_t\right)^2}{k}} = \pm\left(V_{GS_{Total}} - V_t\right) \tag{7.35}$$

Currents i_{d_+} and i_{d_-} are depicted in Fig. A.4. In this figure the horizontal scale is normalized to $\left(V_{GS} - V_t\right)$ corresponding to the *overdrive* voltage of both transistors in the equilibrium situation. Therefore, for values of $v_i \geq \sqrt{2} \cdot \left(V_{GS} - V_t\right)$ all the current will flow on the right side of the differential pair, and for $v_i \leq -\sqrt{2} \cdot \left(V_{GS} - V_t\right)$ all the current will flow on the left side of the differential pair.

The differential output voltage $v_O = v_{O+} - v_{O-}$, is given by:

$$v_O = \left(V_{DD} - R_D \cdot i_{d_-}\right) - \left(V_{DD} - R_D \cdot i_{d_+}\right) \quad \Rightarrow \quad v_O = -R_D \cdot \left(i_{d_+} - i_{d_-}\right) \tag{7.36}$$

$$v_O = -R_D \cdot \left(\frac{I}{2} - v_i \cdot \sqrt{k} \cdot \sqrt{\frac{I}{2} - \frac{k \cdot {v_i}^2}{4}} - \frac{I}{2} + v_i \cdot \sqrt{k} \cdot \sqrt{\frac{I}{2} - \frac{k \cdot {v_i}^2}{4}} \right) \tag{7.37}$$

for $\left| v_i \right| \leq \sqrt{2} \cdot \left(V_{GS} - V_t\right)$, i.e. for $\left| v_i \right| \leq \sqrt{\frac{I}{k}}$, the output voltage is given by:

$$v_O = v_i \cdot R_D \cdot \sqrt{2k \cdot I - k^2 \cdot {v_i}^2} \tag{7.38}$$

For $v_i \geq \sqrt{2} \cdot \left(V_{GS} - V_t\right)$ the differential output voltage $v_O = R_D \cdot I$, and for $v_i \leq -\sqrt{2} \cdot \left(V_{GS} - V_t\right)$ the differential output voltage $v_O = -R_D \cdot I$. Fig. A.4 illustrates the

behaviour of the output voltages a function of the input differential voltage for the differential pair in MOS technology.

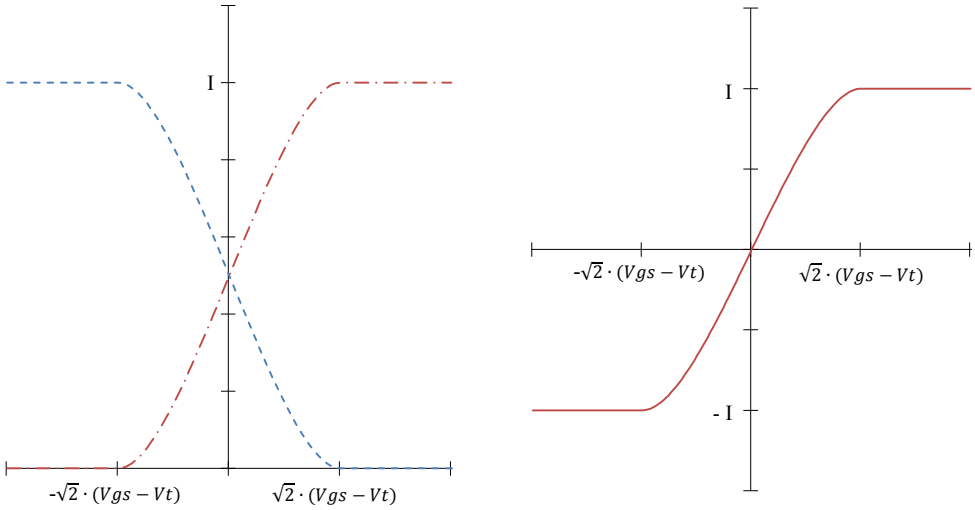

Fig. A.4 – Current output of an ideal differential-pair transconductor.

Annex B: Bandgap voltage reference

Bandgap voltage reference (BG004)

A bandgap voltage reference is a common circuit in semiconductor technology. It yields an output voltage of approximately 1.25V independently of temperature, supply voltage, and process variations of transistors and resistors. The basic circuit is a well-known [B.1], OPAMP based, using two bipolar devices (implementing two diodes) with an emitter area ratio of approximately 1:10. This circuit uses the difference between the voltage of the bipolar junctions to generate the PTAT (proportional to absolute temperature) current, that in turn cancels the first order temperature variation off the bandgap voltage reference.

For this project, a bandgap reference was designed in ATMEL's ECAT05 technology to be included in ATMEL/ES2 design kit analog library cells as an available block. The proposed circuit is based on Song's [B.2] as shown in Fig. B.1, where BG_ON is the switch on node and VBG is the output voltage. The main difficulty in this design was the implementation of the diodes in standard CMOS digital technology [B.3]. For this purpose, lateral bipolar PNP devices where used capable of achieving very high β (super-β). This is realized using small width base devices, two versions where realized, one using 1μm width base PNP transistors and other using 0.7μm width base devices.

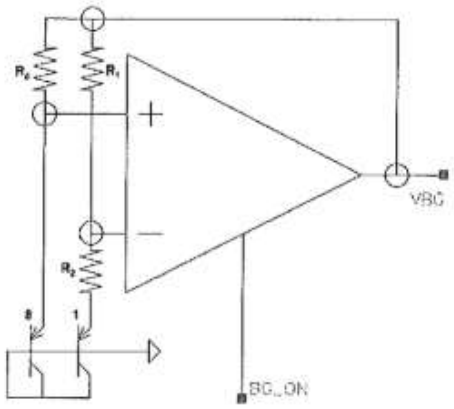

Fig. B.1 – Bandgap voltage schematic (BG004).

In either case the ratio used was 4:32 keeping the basic ratio (1:8) but avoiding the dependence on a single device for increased yield in fabrication as shown in the layout of the BG004 cell depicted in Fig. B.2.

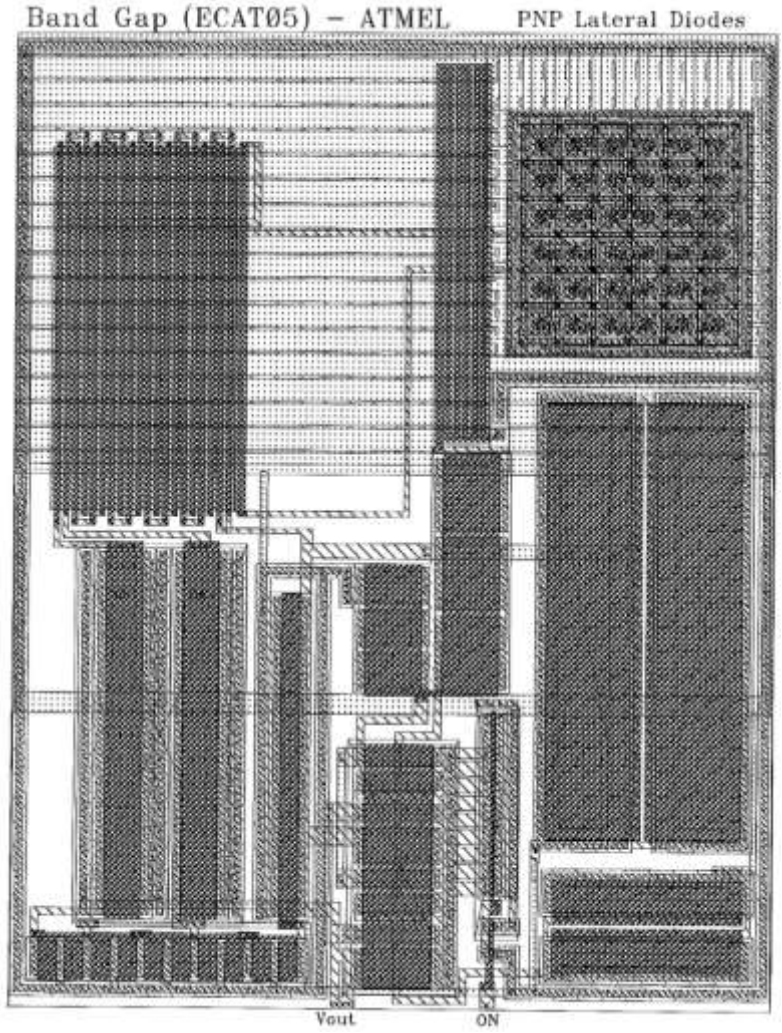

Fig. B.2 – Layout of the bandgap reference (0.7µm device).

Both devices where tested at Rousset foundry on a multi-purpose test wafer with 28 samples (using maximum die size). Fig. B.3 represents the value of the bandgap voltage obtained in all the samples.

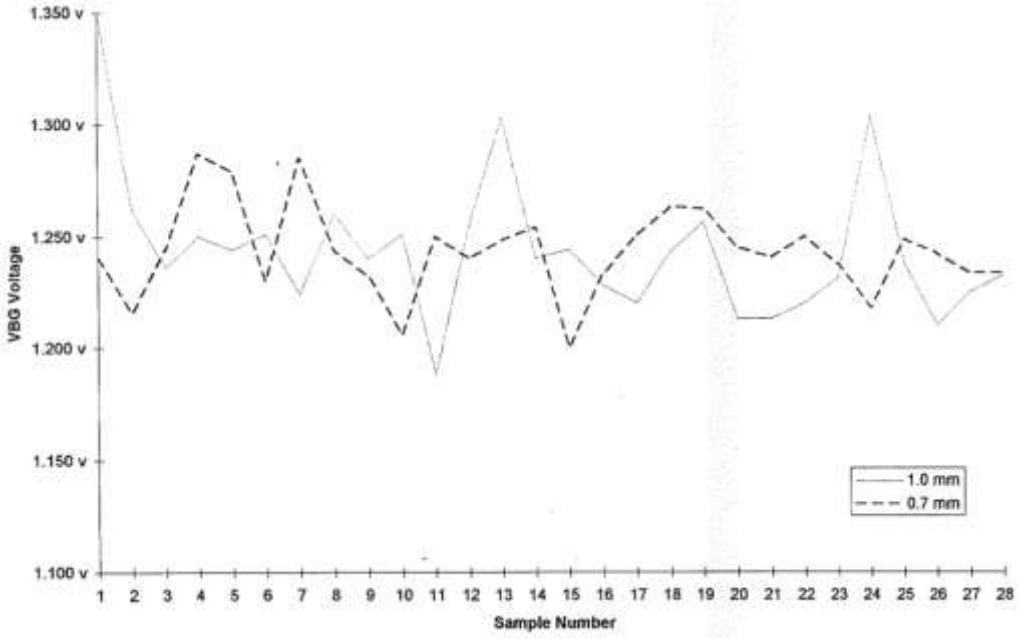

Fig. B.3 – Bandgap reference voltage of all samples.

The layout distribution of the samples and the corresponding measured voltage bandgap voltage values are shown in figures Fig. B.4 and Fig. B.5, respectively for 0.7μm and for 1.0μm devices.

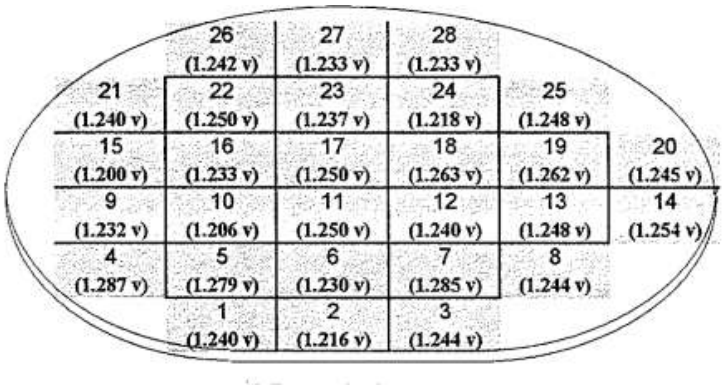

Fig. B.4 – Bandgap reference voltage of 0.7μm bipolar device.

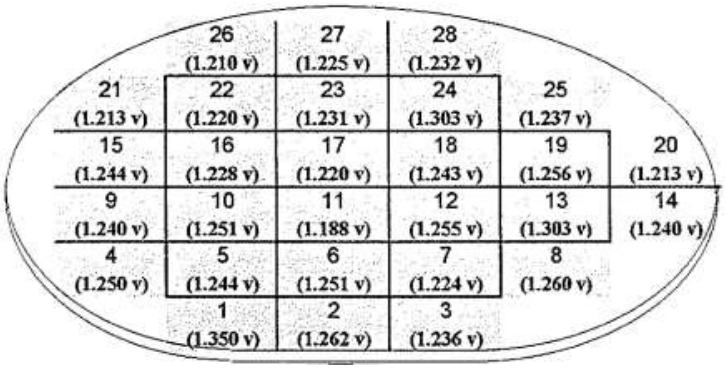

Fig. B.5 – Bandgap reference voltage of 1.0μm bipolar device.

We chose three samples in each design to characterize the voltage to temperature variation figures. In both cases the values chosen where the ones closer to the expected value for the nominal bandgap output voltage. Samples 10, 12, 18 for 1μm devices and samples 19, 20, 23 for 0.7μm devices show good nearly flat figures as depicted in Fig. B.6. The values for output voltage variation versus temperature are under 10ppm/ºC (approximately half of the desired specification for the cell).

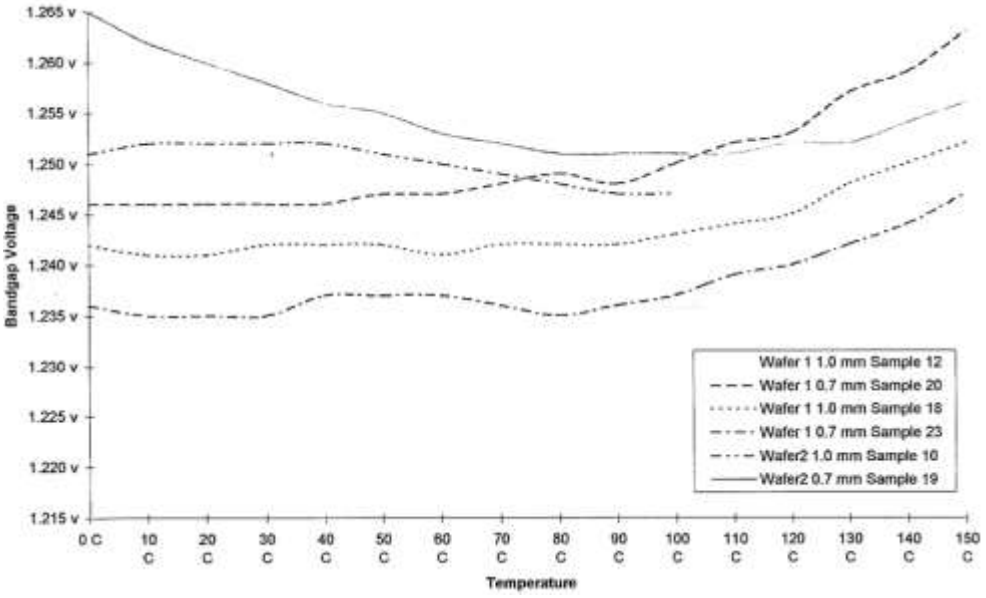

Fig. B.6 – Bandgap voltage versus temperature of samples 10, 12, 18 (1μm) and of samples 19, 20, 23 (0.7μm).

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